Designing with DrMOS
Part II: Application Guidelines

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Traditionally in synchronous buck designs, the PWM controller and its driver have been a single unit, for cost and space considerations. The downside was that the PWM IC with the most desired features did not always come with the most powerful driver. Nor was it possible to closely match that one driver to different power devices. DrMOS offers a logical solution to the problem, putting all the unintelligent components of the buck converter in one package. Co-packaging the driver with two MOSFETs has its challenges but gives a great deal of flexibility to designers, who can derive a logic level PWM signal from anywhere in their system.

Since PWM signal is provided from an external controller or a digital processor extra care must be taken during start up. DrMOS modules must be powered up and enabled before the PWM input is applied. It should be ensured that PWM signal is applied through a proper soft start sequence to minimise inrush current in the converter. Powering the module with a full duty cycle PWM signal already applied may lead to a number of undesirable consequences. If the DISB# is used similar caution is necessary to ensure proper sequencing with the PWM controller. Every time the power module is disabled through DISB# there will be no output and the external controller may enter into open loop and put out a PWM signal with maximum duty ratio possible. If the DrMOS is re-enabled by simply taking DSBL# high, there will be extremely large inrush currents while the output voltage builds up again which may drive the system into current limit. There might be unpredictable consequences such as inductor saturation, overloading of input or even a catastrophic failure of the device. It is recommended that PWM controller be disabled whenever the DrMOS power stage is disabled or non operational for any reason. PWM controller should always be enabled with a soft start to minimise stresses on the converter.

Module Loss and Efficiency

Intel Rev 3.0 specifications impose fairly stringent limits on module loss and efficiency on DrMOS power trains. Under the specific boundary conditions of 12Vin / 1Vout / 25A (28A max) with operating frequency of 300 kHz to 1 MHz, the target for module losses is 6W maximum. The actual performance of AOZ5006 is shown in *Fig. 5*.

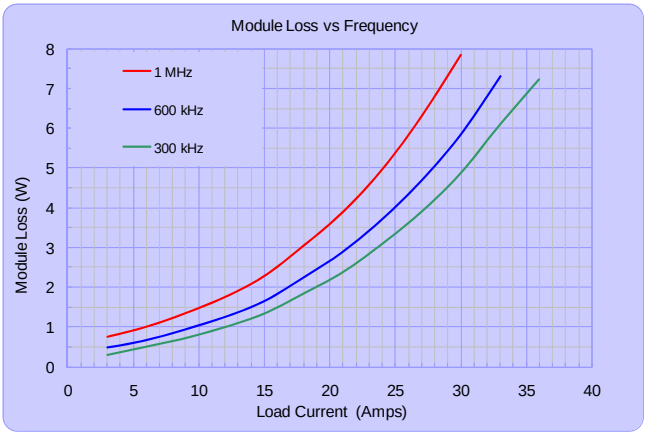

Fig. 5. Module loss vs switching frequency
(VIN = 12V, VDRV = 5V, Vout = 1.2V, Lout = 470 nH.)

As with any SMT power device the so called “rated current” of a DrMOS module is no indicator of its performance[4]. It is misleading at best, and provided more for specmanship than as a usable design parameter. Designers should instead look carefully at the projected module losses specified at their operating conditions. Datasheets give only typical values of these losses so a derating factor needs to be applied. If at all a rated current must be assigned, and there is absolutely no technical reason for doing it, look at the output current value at a loss of 6W. This is the limit set by Intel DrMOS specifications under all operating conditions. Most devices can deliver only 27-28A at 300 kHz within this power limit though their datasheets tout 35A current capability. The module loss for AOZ5006 is below 5W at 30A and 300 kHz as seen in *Fig. 5*.

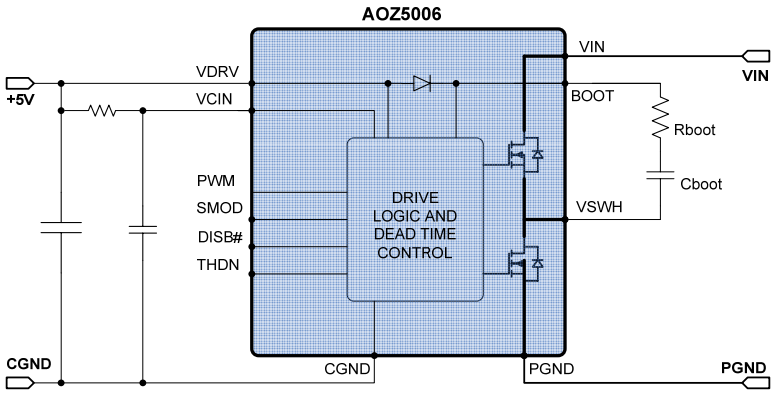

Fig. 6. Connecting cboot and rboot for high side gate supply

Using Rboot

The boost supply for driving the high side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node VSWH. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 4 and 15. Boost diode is integrated into the package. *Fig. 6* shows Rboot, an optional resistor used by many designers to slow down the turn on speed of the high side MOSFET. The value is a compromise to keep both the switching time and VSWH node spikes as low as possible and is typically 1Ω ~ 10Ω. *Fig. 7* shows the impact of various values of RBOOT on VSWH voltage at VIN = 12V, VOUT = 1.2V @ 30A. The curves have been off set by 5 ns to get a clear picture. As RBOOT value is increased the switching speed reduces and both peak voltage and ringing are reduced. However there is a penalty of nearly 0.4W in module losses from 1.5Ω to 20Ω. RBOOT does not impact the turn off speed of the HS FET.

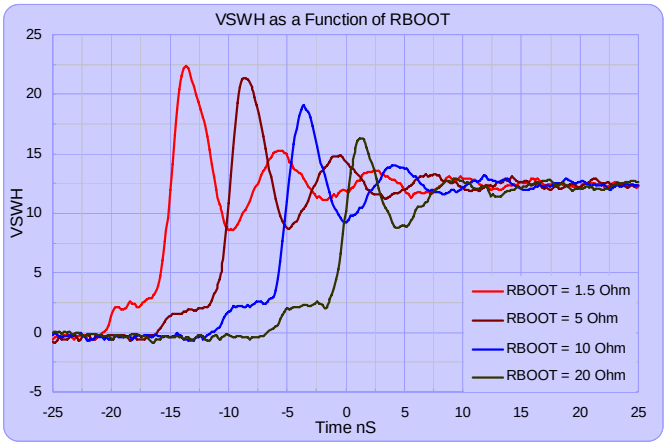

Fig. 7. VSWH vs RBOOT resistor

Balancing the Losses

DrMOS manufacturers try to ensure that HS and LS FET temperatures are evenly matched for its most common application – converting 12V input to a low voltage at several hundred kHz. Obviously the matching will not hold under other operating conditions, in which case the hotter junction will define operating limits. For example when the module is operated at low VIN and/or higher output voltages, the duty ratio will be higher. A trade off is already in place in the HS FET RDSON value for reducing the switching losses and its conduction losses will increase. This will be compensated to some extent by lower losses in the LS FET. The losses have not been eliminated; merely transferred to the HS FET which has a smaller die. Since the two MOSFETs have their own exposed pads and PCB copper areas, the HS FET may become disproportionately hotter than the LS FET. For any application it is necessary to calculate the losses in each device and ensure that temperature rise is within design and derating guidelines. Note that it is the junction temperatures that need to be matched, not losses. During prototyping it is strongly recommended that worst case temperatures be measured and ensured to be within safe limits.

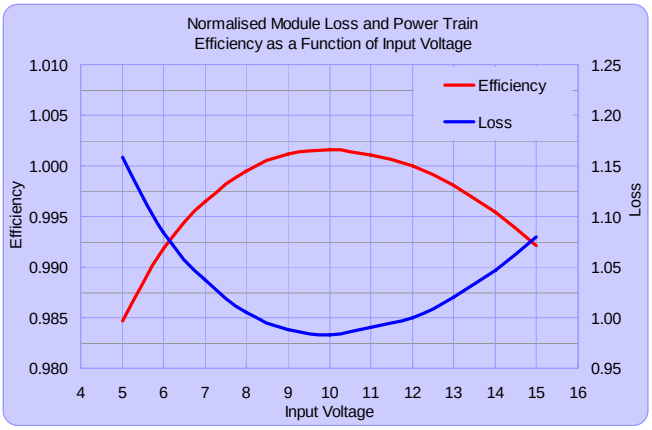

Fig. 8a. Normalised module loss vs input voltage

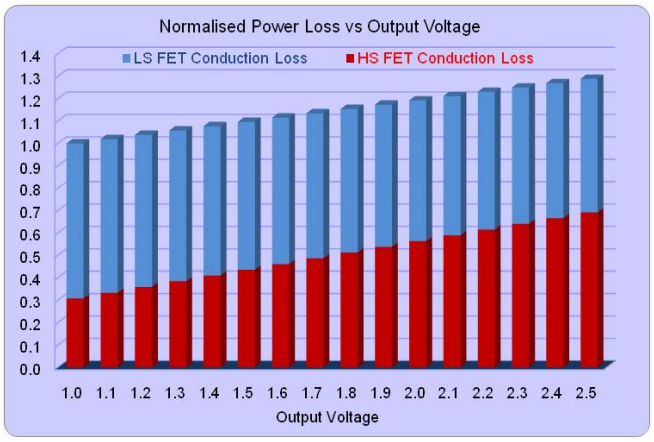

Fig. 8b. Normalised module loss vs output voltage

Fig. 8a shows the variation in module loss as a function of input voltage, keeping output voltage and load constant. From 10V down to 5V of input, total losses increase as much as 20%, bulk of it is additional conduction loss incurred by the HS FET. *Fig. 8b* shows the loss distribution when the input voltage and output current are constant but output voltage is varied. The values are normalised using total conduction losses at Vout = 1V as reference. As the output voltage is varied from 1V to 2.5V, the total conduction losses rise by nearly 30%. While the efficiency of the converter will look impressive, individual temperature rises could be far from acceptable. In the above example LS FET conduction losses are reduced by barely 15% but HS FET losses have more than doubled.

PCB Layout and Thermal Design

AOZ5006 is a high current module rated for operation up to 1 MHz at 25A or higher. This requires extremely fast switching speeds to keep the total losses and device temperatures within limits. Excellent switching speeds are achieved by a robust gate driver integrated within the package, but correspondingly high levels of dv/dt and di/dt will be observed throughout the power train. Careful attention to PCB layout will help minimise voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimise the area of the primary switching current loop, formed by the HS FET, LS FET and the input bypass capacitor Cin. The PCB design is somewhat simplified because of the optimised pin out in DrMOS. As can be seen in *Fig. 9*, the bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS FET, output inductor and output capacitor Cout is the next critical parameter. The ground plane should be extended and the negative pins of Cout should be returned to it, again as close as possible to the device pins.

While AOZ5006 is extremely efficient it is still required to safely dissipate up to 6W of heat in a tiny package measuring 6 mm x 6 mm. This requires careful attention to thermal design particularly if all heat must flow out through the PCB. DrMOS package has been well defined to get the maximum heat out of the devices. AOZ5006 takes it one step further with an all clip construction. Both MOSFETs are directly attached to individual exposed pads. This allows individual copper pours and good thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. An inner power plane layer dedicated

to VIN, typically the 12V system input, is desirable and vias should be provided near the device to connect the VIN copper pour to the power plane. AOZ5006 uses a large clip to make the PGND connections on the LS FET. Though ground does not form a part of any device tabs, significant amount of heat is dissipated though the clip into multiple PGND pins. A large copper pour connected to PGND pins and to system ground plane will further improve thermal management. *Fig. 9* illustrates the various copper pours and bypass capacitor locations.

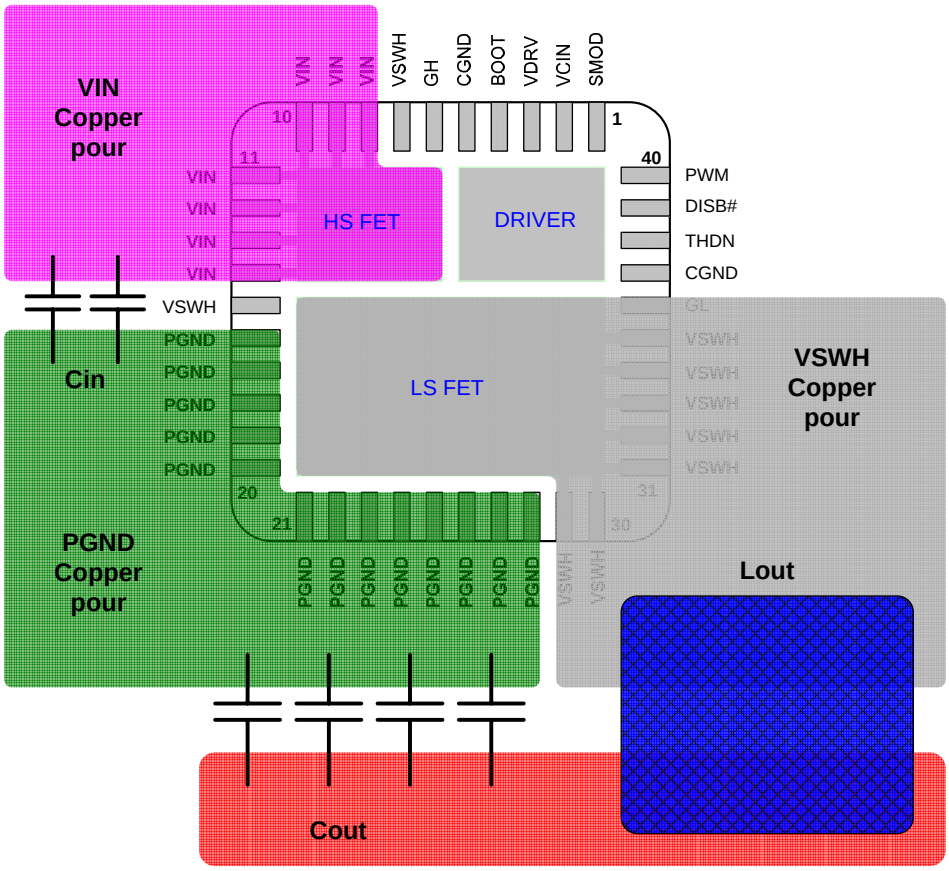

Fig. 9. PCB layout illustration for minimising current loops

Top Side Cooling Options

In multi phase designs several DrMOS modules will be located in a small area of the PCB, making it difficult to provide large individual copper pours. Some form of top side cooling may be a good option in such cases. Obviously the plastic mold compound is not a good conductor of heat, but DrMOS modules are quite thin, less than 1 mm in profile. Height permitting, a finned heatsink attached to a group of modules can provide an additional channel for the heat to flow out.

The thermal resistance from junction to top surface is not easy to measure accurately, no standard methods exist in the industry. In case of DrMOS, the presence of two devices with different losses and different junction temperatures further complicates the specifications. Preliminary evaluation at AOS indicates that the junction to surface thermal resistance $R_{\theta js}$ is in the range of 10-12 ^{o}C/W for the package. While higher than the $R_{\theta jc}$ of 5 ^{o}C/W, it is still quite low for a plastic surface and a result of special construction features. All power connections in AOZ5006 are done with copper clips on both sides of the die to reduce the resistance and inductances associated with bond wires. In addition to minimising parasitics, the large top side clips also provide a low resistance thermal path to the surface through a thin layer of mold compound. However, top cooling comes with a number of caveats.

1) $R_{\theta js}$ measurements were made under specific conditions where both junctions are approximately at the same temperature, about 40 ^{o}C above the surface.

2) There will be an additional 2-3 ^{o}C/W of thermal resistance from the plastic surface to the metallic heatsink.

3) Most important, top cooling is not a substitute for heat dissipation through the PCB. For example if only top side cooling were used at an ambient of 50 ^{o}C and the device dissipates 5W, an infinite heatsink will be required to keep Tj <= 125 ^{o}C in the worst case.

What really matters is the effective thermal resistance from junction to ambient through all available paths. A dedicated heatsink attached to the top will have much lower thermal resistance to surrounding air and will help to reduce not only the junction temperature but also that of the PCB.

References:

4) Havanur, Sanjay "Forget Power Device Current Ratings, Calculate Application Losses" Power Electronics Technology, Feb 2010, pp 16-19. Available online at http://powerelectronics.com/power_semiconductors/power_MOSFETs/forget-power-device-current-ratings-022010/