High-frequency and high-density design of all GaN power supply unit

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Abstract

The GaN FETs have the capability of faster switching and lower on resistance than Silicon FETs. In many cost and space sensitive applications, GaN FETs can achieve high power density solution. This paper presents the design of high frequency high efficiency all GaN FETs solution for 240Vac to 48Vdc 3.2kW power supply unit (PSU). The PUS consists of an interleaved totem pole power factor corrector (PFC) with triangular current mode (TCM) and a LLC resonant converter. Zero voltage switching (ZVS) can be achieved for both PFC and LLC converter which increase the PSU switching frequency as well as power density.

1. Introduction

In 2014, data centers in the U.S. consumed an estimated 70 billion kWh, which is believed to be 1.8% of total U.S. electricity consumption [1]. The energy usage for data centers is expected to continuous increase in the future. Based on current trend estimates, U.S. data centers may consume approximately 73 billion kWh in 2020.

There is increasing demand for better space utilization in the data center and today's 15 kW rack will soon consume up to 60 kW. Higher efficiency and power density power supply units become inevitable not only to lower the data center electric bill but also allow more power and servers per rack. The 240Vac to 48V power delivery are widely used in todays' rack architecture. The PSU consists of an interleaved totem pole power factor corrector (PFC) with triangular current mode (TCM) [2] and a LLC resonant converter with synchronous rectifiers [3] as shown in Fig. 1. Zero voltage switching (ZVS) can be achieved for both PFC and LLC converter which enable the increasing of the switching frequency as well as power density.

Enabled by about 10 times higher critical electric field and 3 times higher channel mobility, lateral GaN E-HEMT have been proven faster switching and lower on resistance comparing to Silicon FET. Combined these with advanced circuit techniques and high performance magnetics, GaN power electronics is entering a new era where ultra-high power density and high efficiency can be achieved at the same time [4].

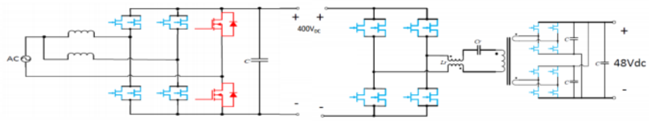


Fig. 1. Topologies of the PSU, which consists of an interleaved totem pole power factor corrector (PFC) with triangular current mode (TCM) and a LLC resonant converter.

2. The triangular current mode (TCM) PFC with ZVS

The PFC is one of those major power delivery circuits that GaN FETs can apply. One of those popular topologies is the hard switching totem pole continuous conduction mode (CCM) hard switching PFC (typically operating fixed frequency below 100 kHz). There is also TCM totem pole ZVS PFC (variable frequency and maximum frequency above 1 Mhz). Comparing to CCM PFC, the TCM PFC has about 33% higher conduction losses due to higher current ripple. However, due to high transfer conductance and the monolithic integrated gate driver with GaN FET, the turn-off switching become fast that turn-off loss can almost be ignored. The total loss can be cut about 33.5% as shown in TABLE 1 (if we assume CMM hard-turn-on is 50% and the conduction is 50% per unit, TCM conduction loss is 50%*133% and 0% on switching). Please also note higher GaN FET loss in CCM PFC caused by hard switching will increase the junction temperature where the enhanced mode GaN FET normally has 1% on-resistance increase per 1 °C. As a result, the on resistance increases and further produces more conduction loss.

TABLE I: loss break down (per unit) between CCM PFC and TCM PFC

	Conduction loss	Switching loss	Total losses
CCM	50%	50%	50%+50%=**1**
TCM	50%*1.33	0	50%*1.33+0=**0.665**

TABLE I is based upon a simplified assumption of 400V/7A turn-on switching with 30uJ turn-on switching loss (100kHz). The switching loss is 30uJ*100kHz=3W. The conduction loss is 7A^2*68mΩ*1.3=3.3W (assuming 55°C junction temperature).

The GaN FETs of TCM ZVS totem pole has the advantage of lower losses. The junction temperature of GaN FETs can be further reduce by optimizing the layout. In the prototype, each phase high side and low side both have two NV6117 GaN FETs (600V 110mΩ) in parallel (4 devices per phase, and 8 devices for 2 phases). The vertical GaN half bridge card was designed to mount on the motherboard. The half bridge GaN cards are 0.8mm thickness with 4 layers 4 oz copper. Large copper area with thermal vias are placed under the thermal pad of NV6117 as shown in Fig. 2. The 6.5mm height heat sink has 4 screws on the corners to fasten to the PCB with a 0.3mm thermal interface.

The PFC inductor is 9.5 uH and the PFC operates from 350 kHz to 1.5 Mhz at full load condition. The inductor is made of two pieces of MS91S Ferrite E32/6/20 core. 10 turns of Litz wire and leg gapping are applied to the prototype PFC inductor.

The detail PFC control was described in the references [2] and [3], where the maximum efficiency 99% can be achieved. The PFC and LLC resonant converter prototype is shown in Fig. 3. The size of the motherboard is 210mm × 81mm*43mm. The power density is 73W/inch^3 without housing/fan.

3. The LLC resonant converter with synchronous rectifiers (SRs)

The LLC converter are one of the most popular topology where a fixed voltage gain application is needed. The all GaN LLC resonant converter uses NV6117 600V GaN FETs and EPC2021 80V GaN FETs. The LLC resonant converter operates at the 550 kHz resonant frequency. The transformer design and optimal layout/control of SRs are the keys to achieve high efficiency and high power density.

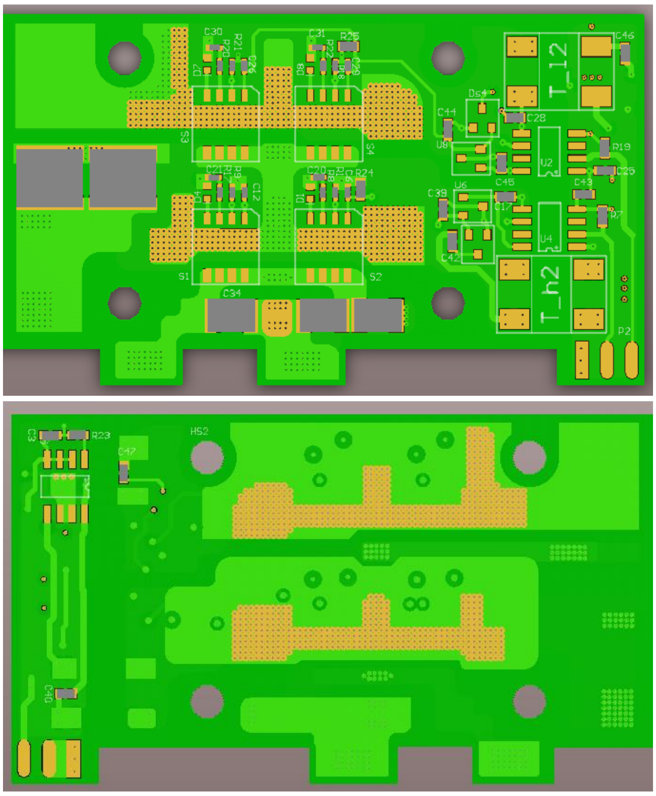
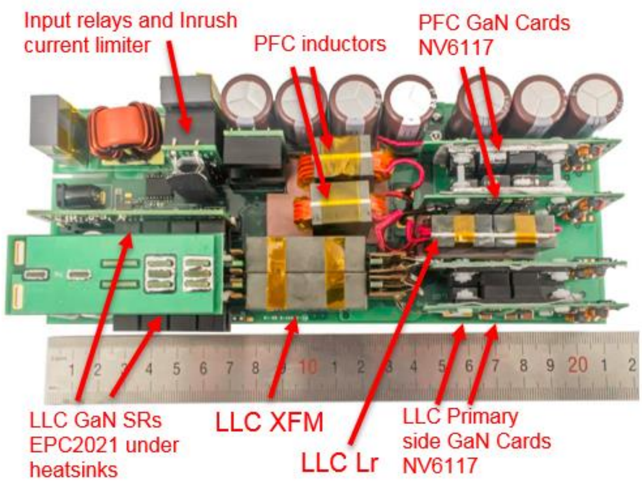


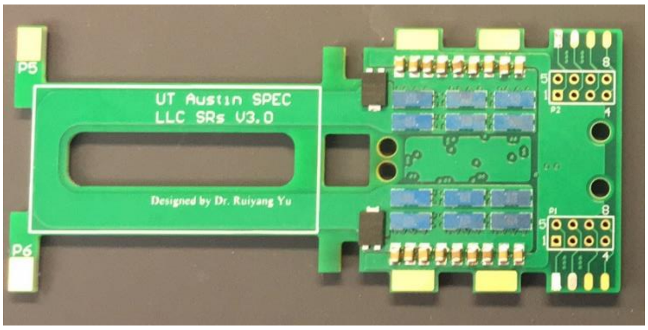
Fig. 2. Top view and bottom view of GaN half-bridge card. Two NV6117 are paralleled for each high side and low side.



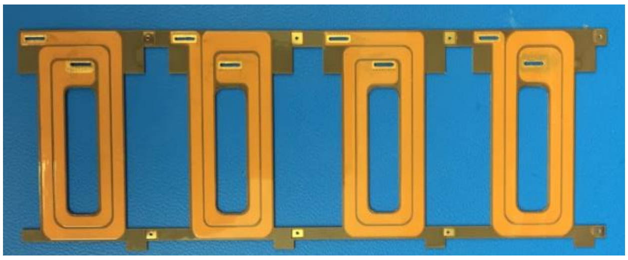
(a) Top view of the 3.2kW PSU prototype

(b) Side view of the 3.2kW PSU prototype

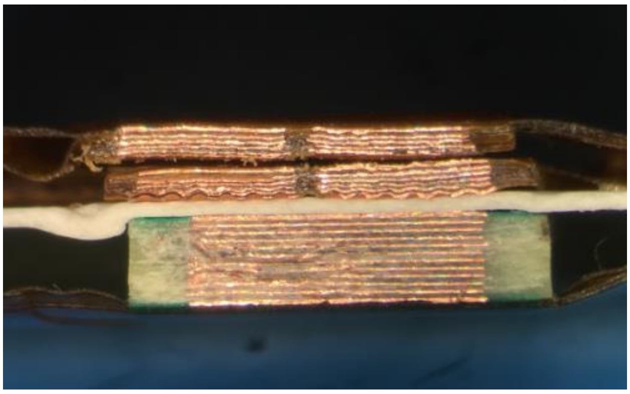
Fig. 3. Prototype of the 3.2kW PSU using all GaN FETs



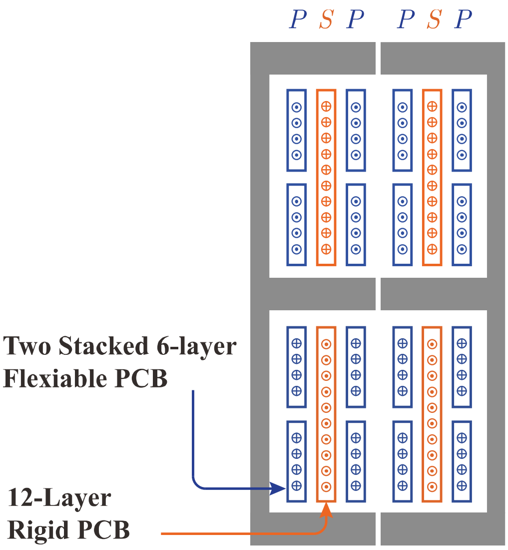
(a) LLC secondary side rigid PCB winding and SRs



(b) 6 layers flexible PCB for primary side winding



(c) Cross section cut microscope view of rigid PCB winding and flexible PCB winding



(d) LLC transformer structure

Fig. 4. The construction of LLC transformer

3.1. Optimal design of LLC transformer

Planar transformer with PCB windings are applied to the design. Comparing the Litz wire transformer, planar transformer has lower AC/DC resistance ratio. Although the PCB winding has lower copper filling factor. Careful design of the transformer structure can still maintain the low DC resistance comparing to the Litz wire design.

The transformer secondary winding is made of 12 layers 1 oz copper rigid PCB with 1.6 mm thickness. The 12-layer is also the maximum number of layer that a standard 1.6 mm rigid PCB can be made. The SRs are also on the same rigid PCB where no solder joints between the transformer secondary winding and the SRs, as shown in Fig. 3 (a).

The flexible PCB winding are used for the primary side winding as shown in Fig. 3 (b). Two stacks of 6 layers 1 oz copper flexible PCB are glued together to form the 12 layers 1.2 mm coil windings.

The cross section cut view of the 12-layer flexible PCB and the 12-layer rigid PCB are shown in Fig. 3 (c).

There is 1 mm spacing between each primary side PCB and secondary side PCB. As a result, the measured coupling capacitance between the primary side winding to the secondary side winding is around 50 pF. The 1 mm spacing can also allow small amount of air flow to go thought the spacing and cooling the windings.

The shape of transformer core is customized made by Hitachi Metal ML95S. There is 1 turn on the secondary side which is designed with 100mT flux swing at 500 kHz resulting core loss 600 to 800 kW/m^3.

Symmetrical layout of the two paralleled SRs cards are also important to balance the current sharing of each SRs card.

3.2. Optimal control of SRs

Since there is double line frequency ripple voltage on the DC link capacitor, the LLC converter will work both below and above frequency. The challenge of SRs timing arises because every nanosecond counts to the diode loss especially the switching frequency is higher than 500 kHz. While conventional voltage sensing based SRs control has a problem on paralleling FETs due to stray inductance issues [5], the current sensing based SRs control are applied to the prototype system [6].

A rogowski coil as shown in Fig. 5 (a) (b) is inserted into the secondary side winding. An integrator is followed by the Rogowski coil to reconstruct the transformer secondary side current signal.

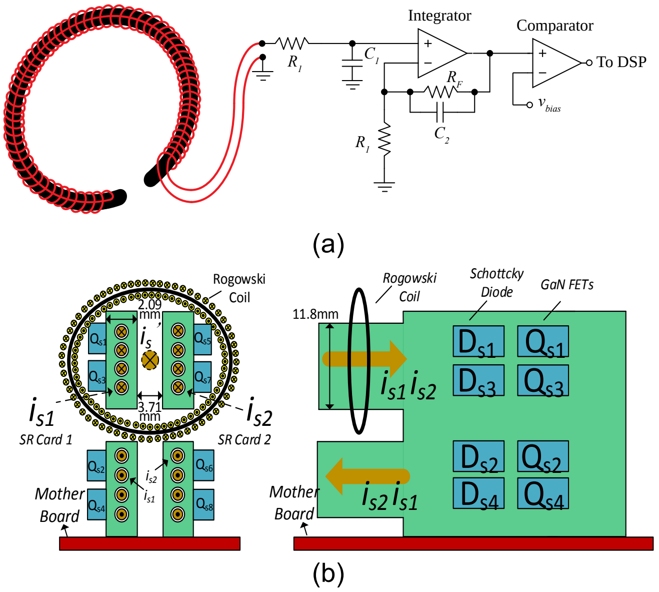


Fig. 5. rogowski coil to implement zero current detection

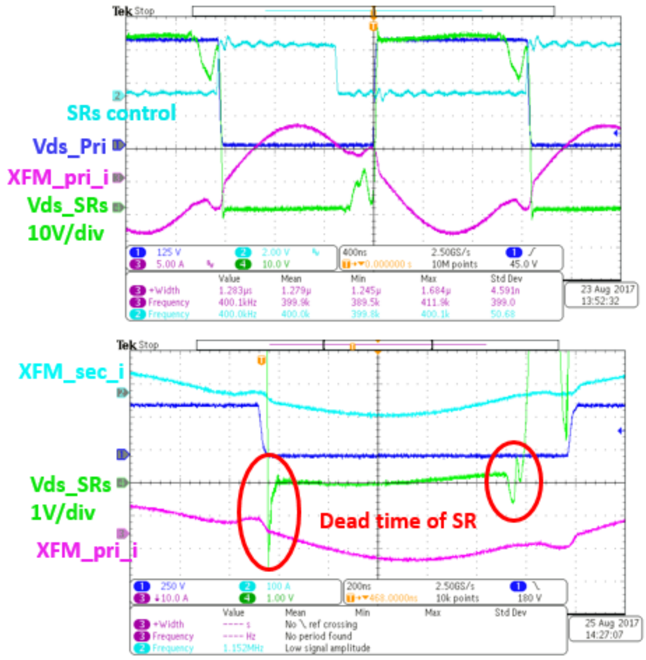


Fig. 6. Waveforms of SRs control

A comparator is used to detect the zero cross of the transformer current. Considering the delay of the driver circuits and noises immunity to prevent false triggering of zero current detection. The microcontroller captures the current zero crossing timing and then determines the SRs timing for the next few cycles rather than the same cycle.

A decision-making algorithm is implemented to identifier the possible false triggering of zero current detection and light load condition of the SRs. The waveforms of the LLC resonant converter are in shown Fig. 6. It has been shown from the waveforms that the dead time of SRs can be controlled less than 30 ns.

The LLC converter maximum efficiency is estimated to be 98.7% which is 0.4% higher than authors previous work presented in [6].

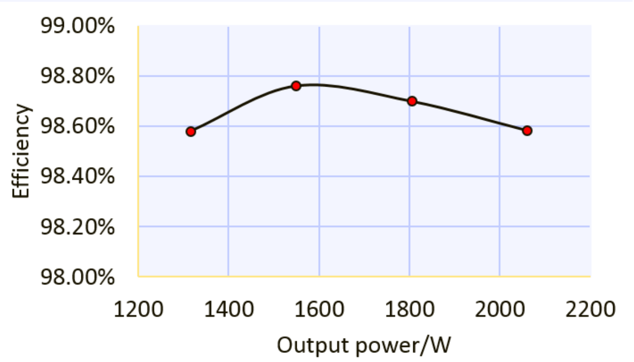


Fig. 6. Estimated LLC converter efficiency

4. Conclusions

The hardware design of the all GaN power supply unit was reviewed in this paper. The dual phase interleaved triangular current mode (TCM) zero voltage switching (ZVS) power factor corrector (PFC) is applied to achieve 240Vac to 400Vdc power conversion. The LLC converter is applied to achieve 400Vdc to 48Vdc with galvanic isolation. The high frequency planar transformer design, the synchronous rectifier control are the keys to achieve high efficiency. The All GaN power supply unit demonstrates the capability of high power density 73W/inch^3 (without housing/fan).

5. References

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