Navitas AllGaN™ Energy, Driven

pcim EUROPE

Navitas

Welcome to the Post-Silicon World:
Wide Bandgap Powers Ahead

May 10, 2016
Nuremberg, Germany

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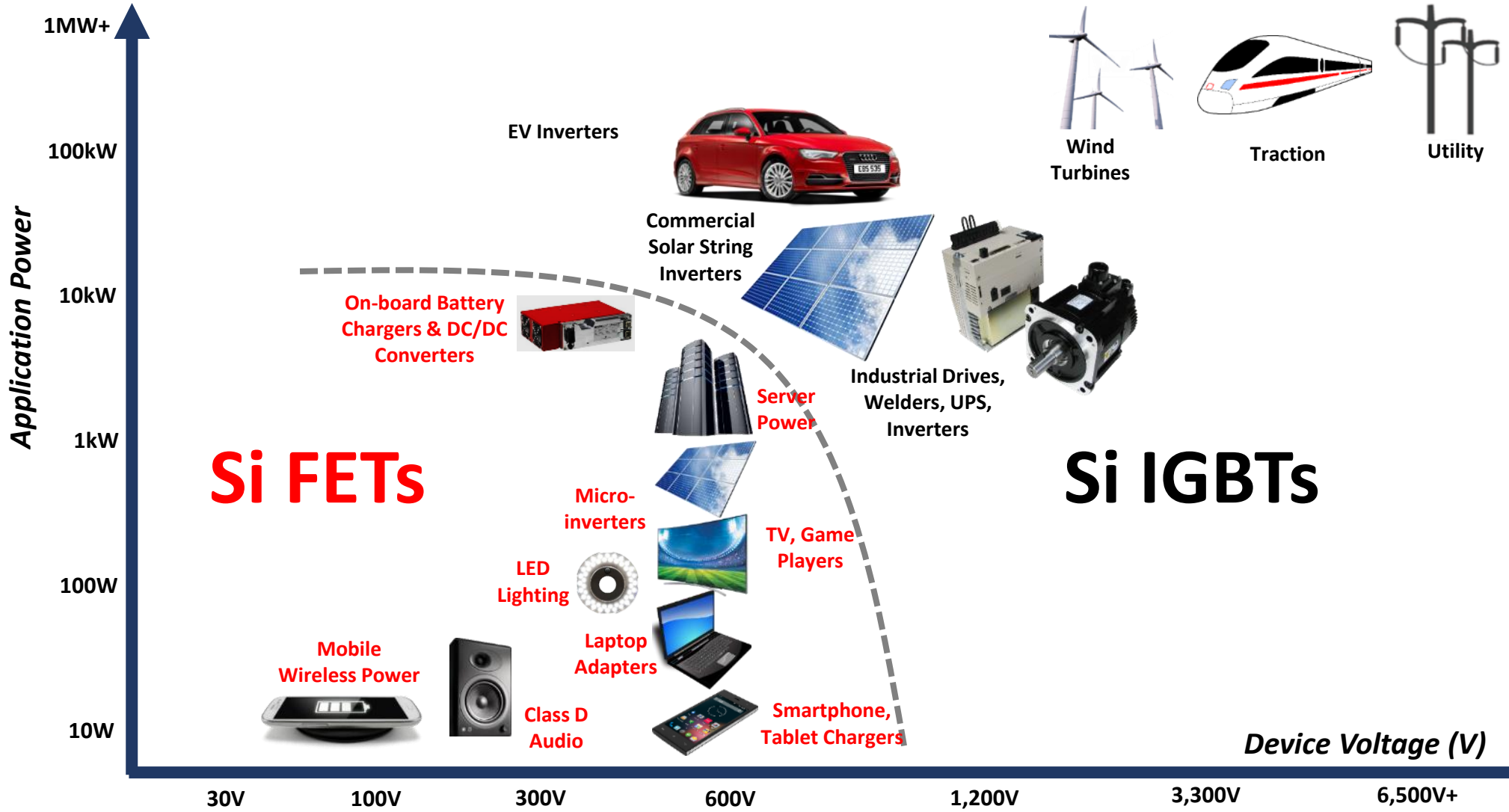
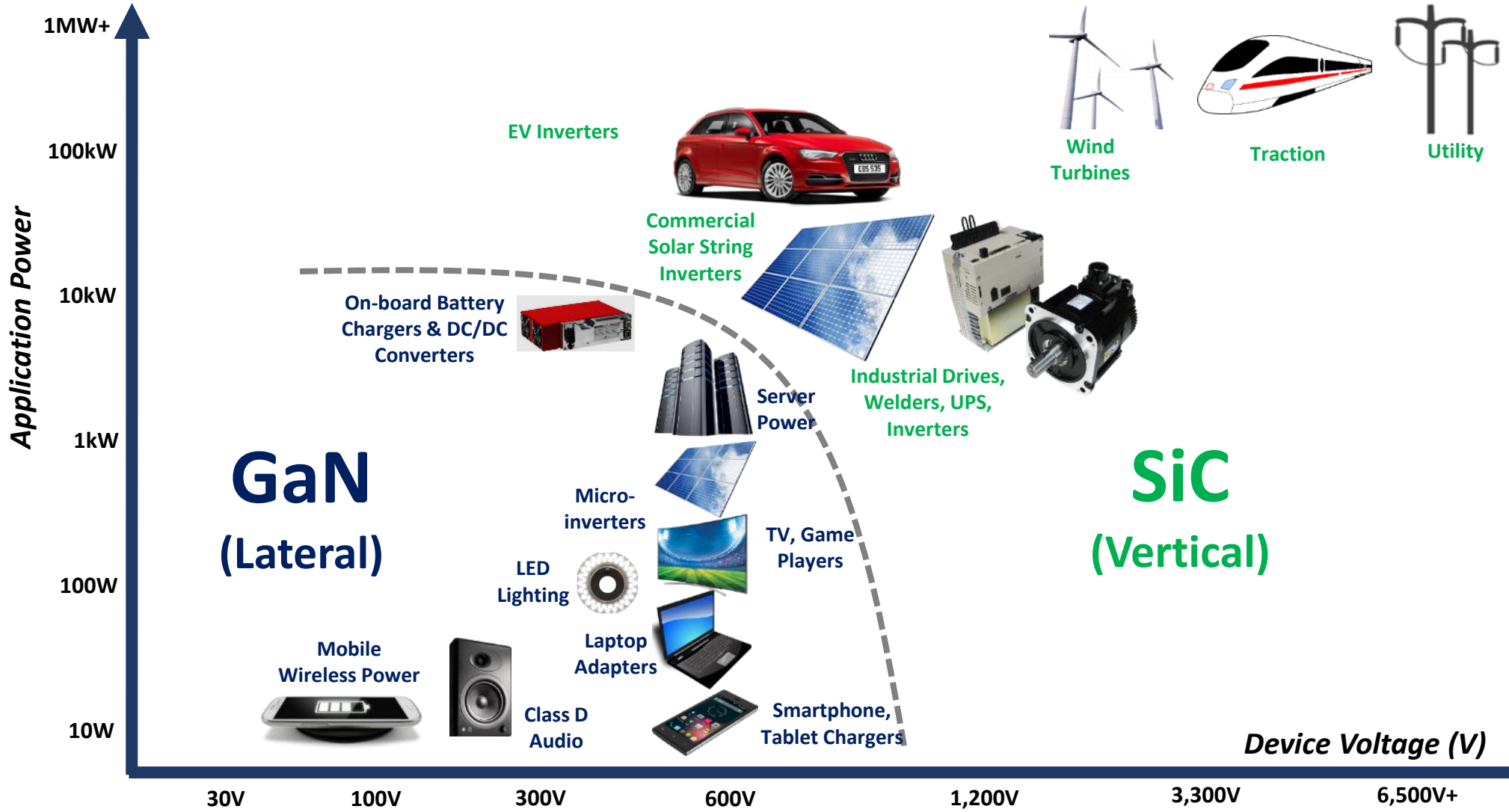
The Si Landscape



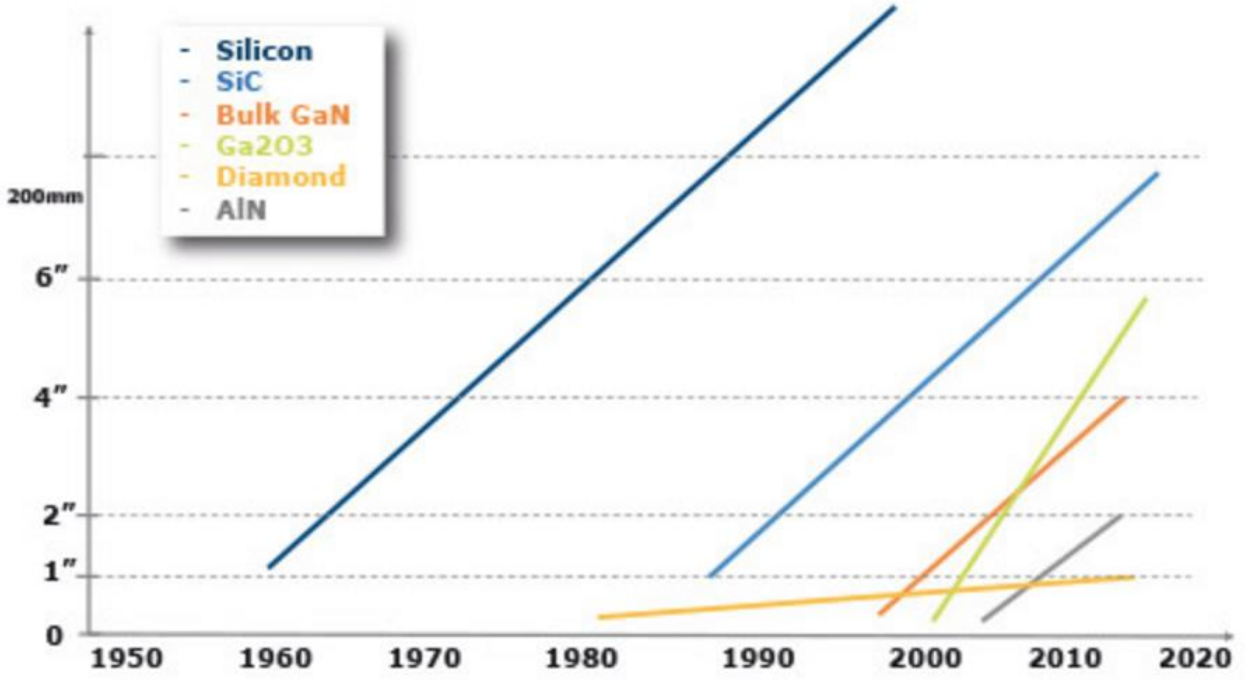
The WBG Landscape



Timeline of Bulk Semiconductor Development

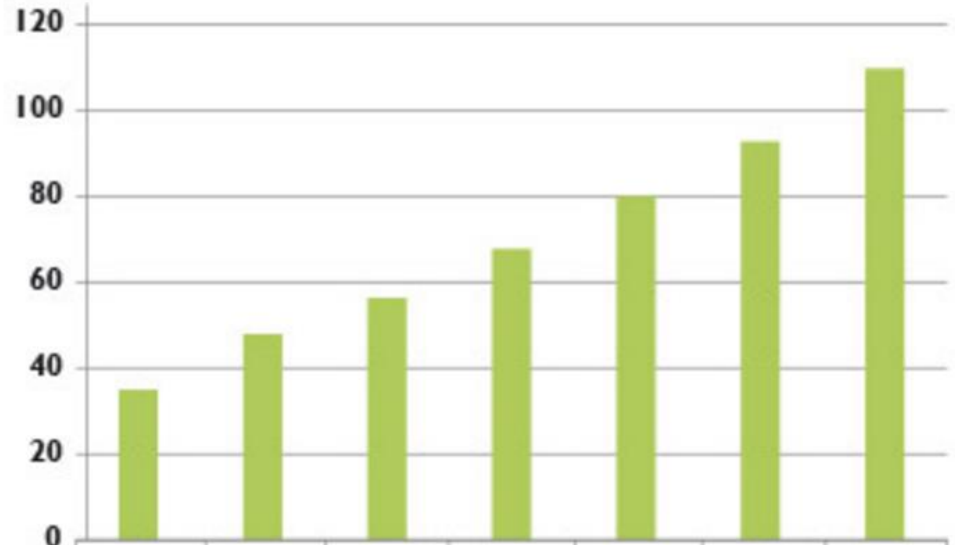
Different crystal diameter expansion

(Source: SiC, GaN, and other Wide Band Gap (WBG) materials for power electronics applications, October 2015)



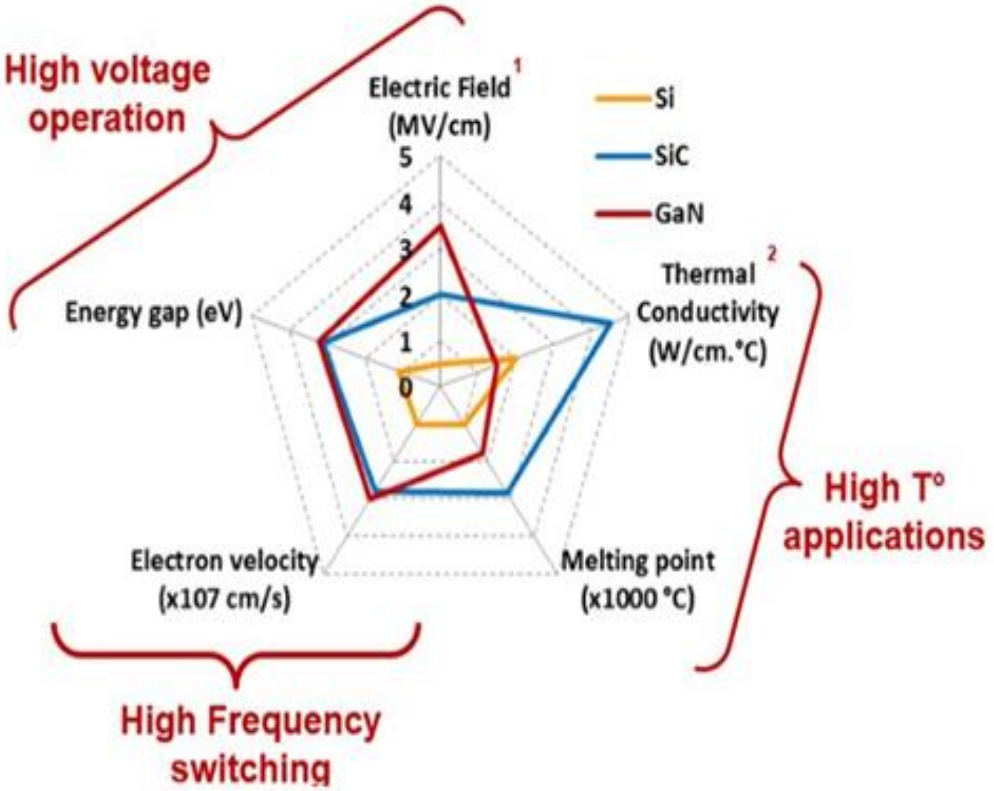
Projected SiC n-type substrate market size ($M) through 2020

(Source: SiC, GaN, and other Wide Band Gap (WBG) materials for power electronics applications, October 2015)

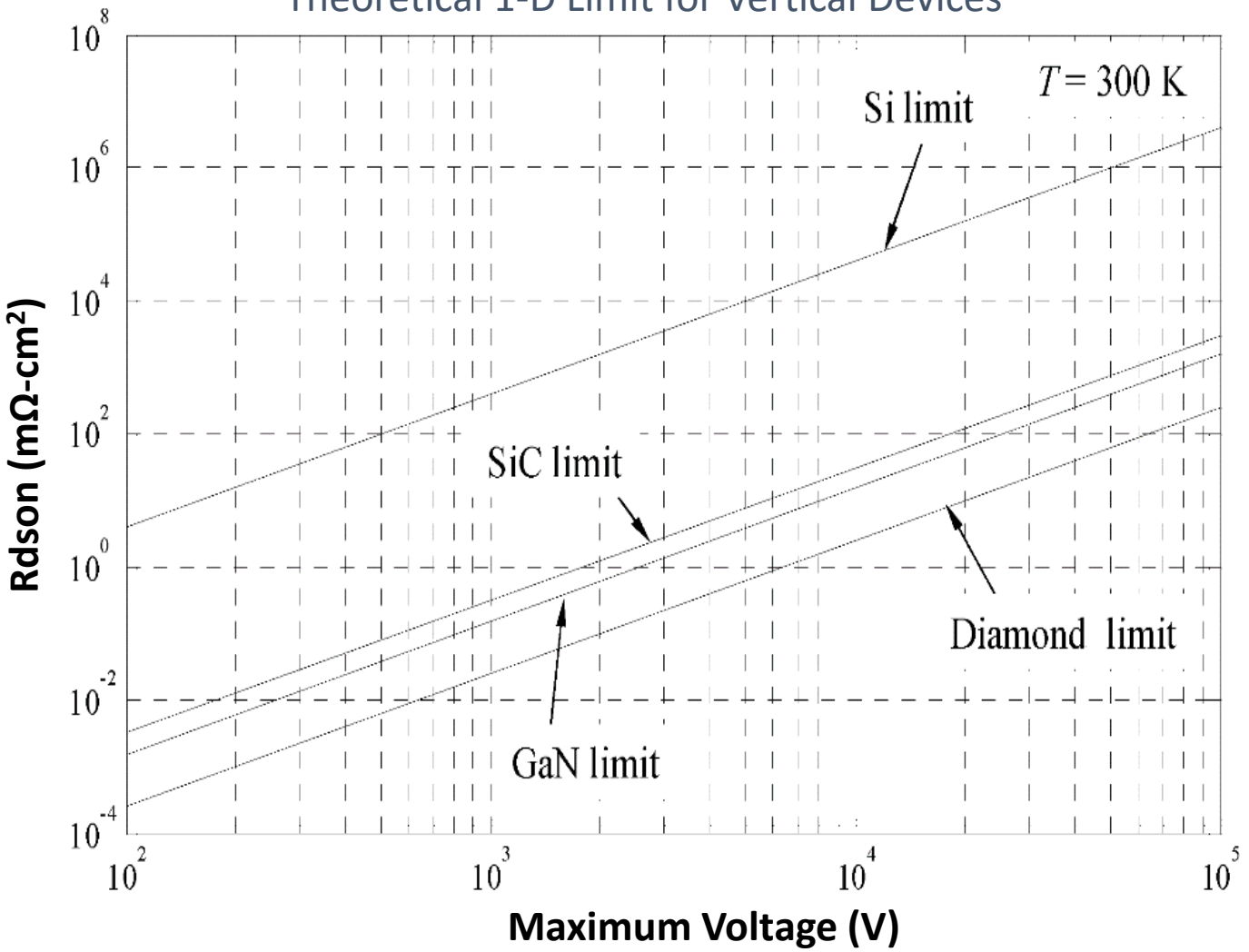


	2014	2015	2016	2017	2018	2019	2020
SiC wafer market size (M$)	35	48	56	68	80	93	110

Performance Limits of WBG Materials

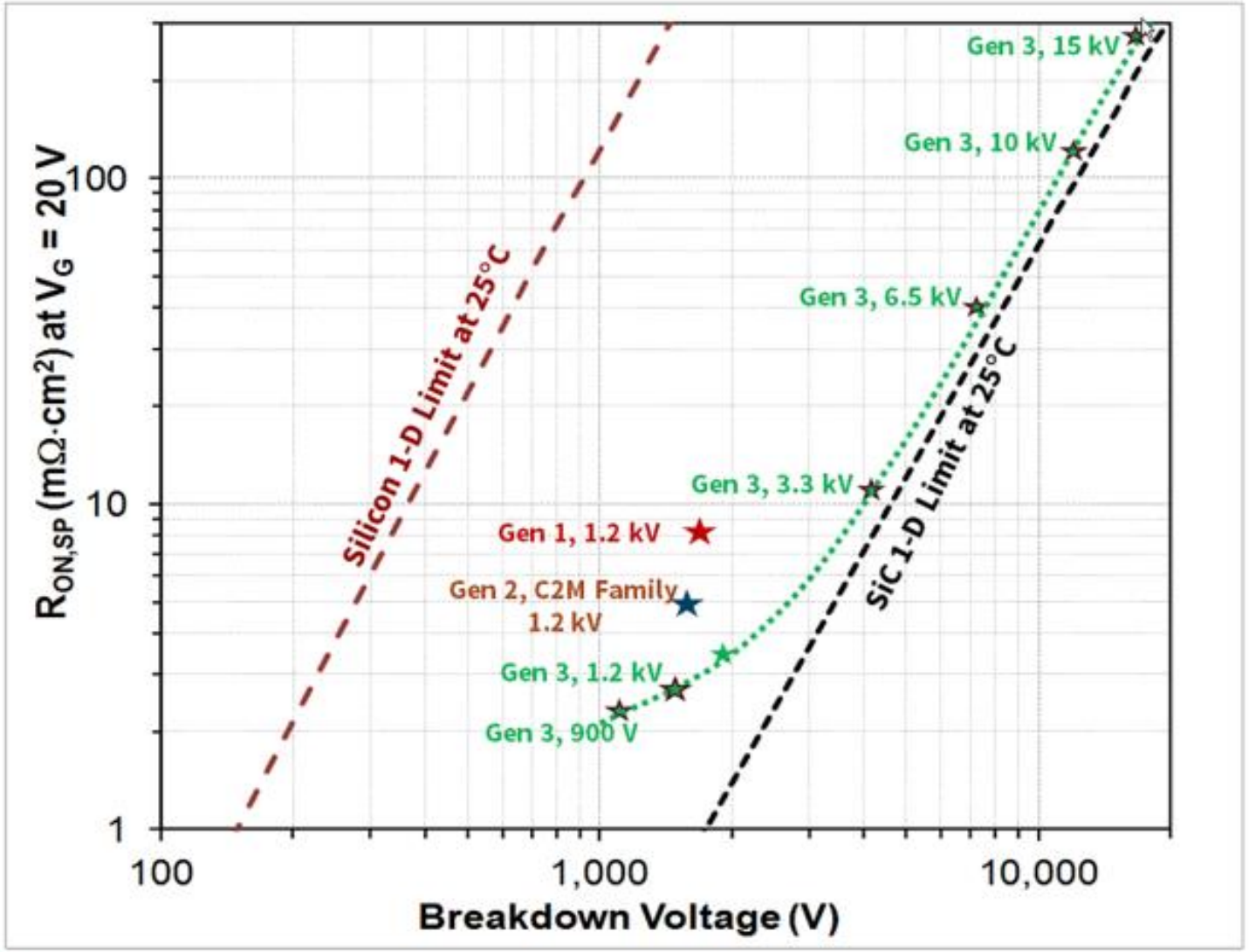


Theoretical 1-D Limit for Vertical Devices



SiC MOSFETs Approach 1-D Theoretical Limit

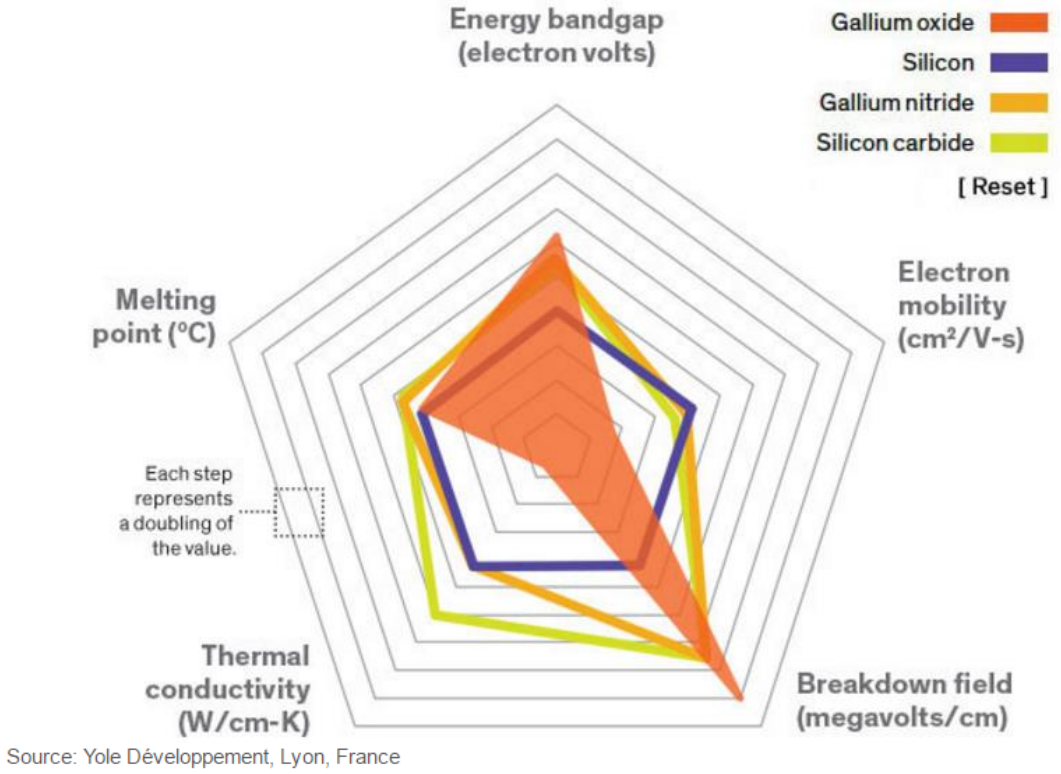
- Latest SiC devices are approaching the 1-D limit across a wide range, even up to 30kV
- At lower voltages like 900V, the gap widens due to channel and substrate resistance
- System cost advantage is possible across the range
- At 900V, SiC MOSFET is reaching cost parity with Superjunction silicon



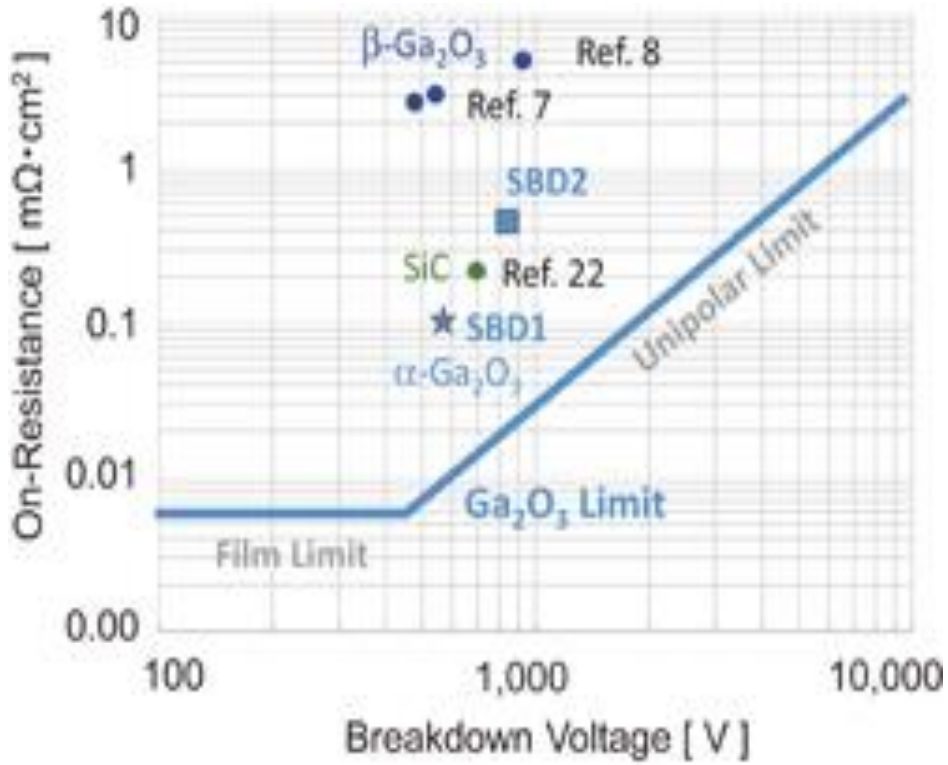
Courtesy of Wolfspeed

A Future HV Alternative to GaN and SiC: Ga_2O_3?

- Flosfia (Kyoto startup), is working to show that Gallium Oxide can be the next big thing in WBG
- Incumbents, and aluminum nitride and diamond players, may not agree!



Source: Yole Développement, Lyon, France



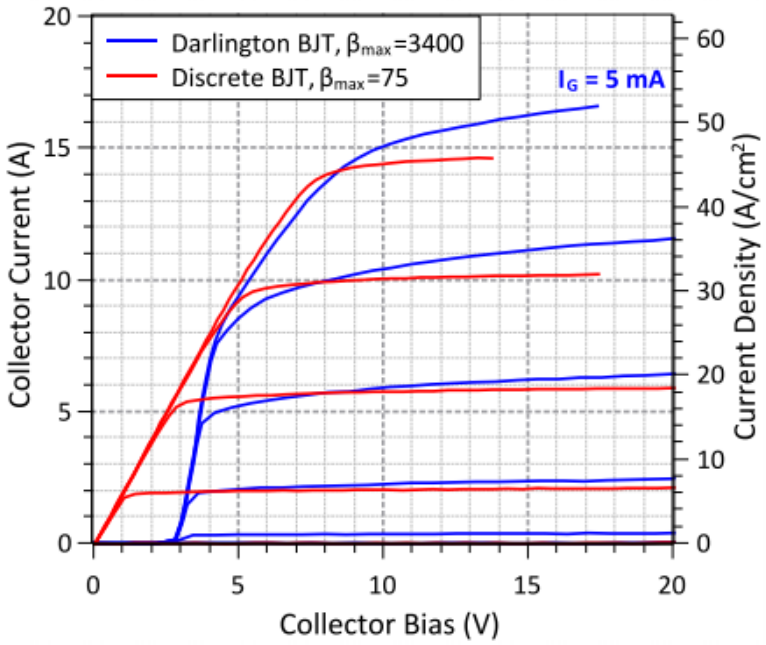
FLOSFIA

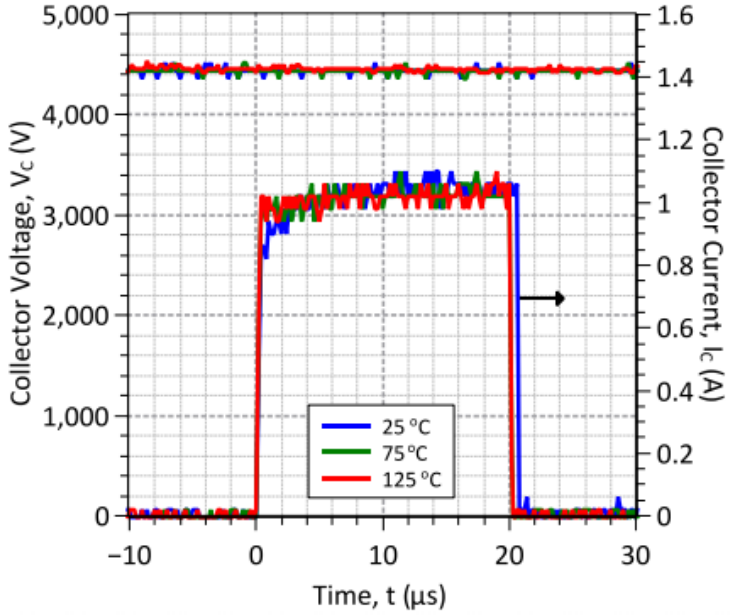
For more: http://flosfia.com/english/ , http://spectrum.ieee.org/semiconductors/materials/gallium-oxide-power-electronics-cool-new-flavor

10kV SiC BJT vs. Si IGBT

- SiC 50% more blocking capability
- On-state voltage higher relative to BV
- 20x faster switching
- With Beta of 75, drive current will be 200mA
- With the Darlington, only 5mA achieves the same voltage drop at maximum load
- Short circuit capability at 4.5kV is greater than 20us, and temperature independent

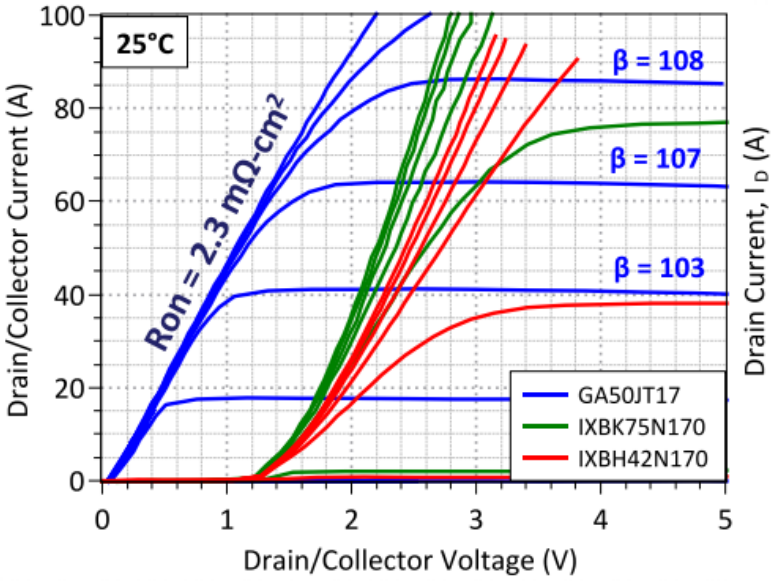
Device	BV	I_C	Temp.(C)	$V_{CE,sat}$ (V)	Eon (mJ)	Eoff (mJ)
SiC BJT	10 kV	8 A	150°C	6.4	4.2	1.6
Si IGBT	6.5 kV	10 A	125°C	4	80	40
				↑ 1.6 x	19 x ↓	25 x ↓

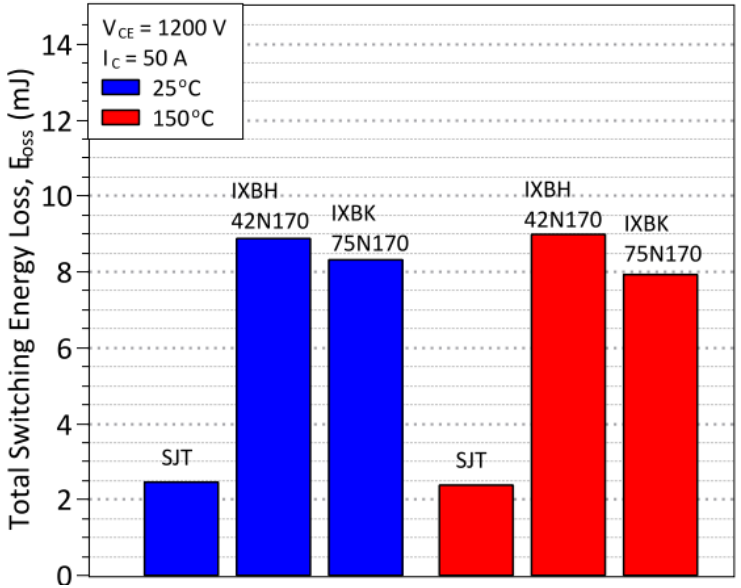


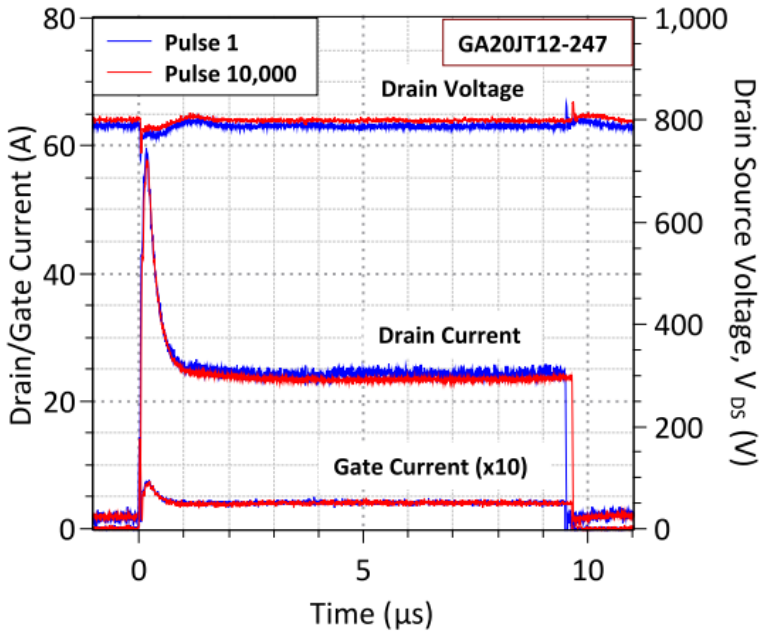


1,700V SiC Junction Transistor vs IGBT

- Best-in-class SiC devices clearly outperform Si IGBTs in all major metrics:
  - Conduction loss down by >50% across temperature range
  - Switching loss down by 75% at full operating voltage with clamped inductive load
  - SOA capability is robust to industry standards, even demonstrated to 10K pulses
  - Hot leakage reduced by 3-4 orders of magnitude (1k -10k x better)



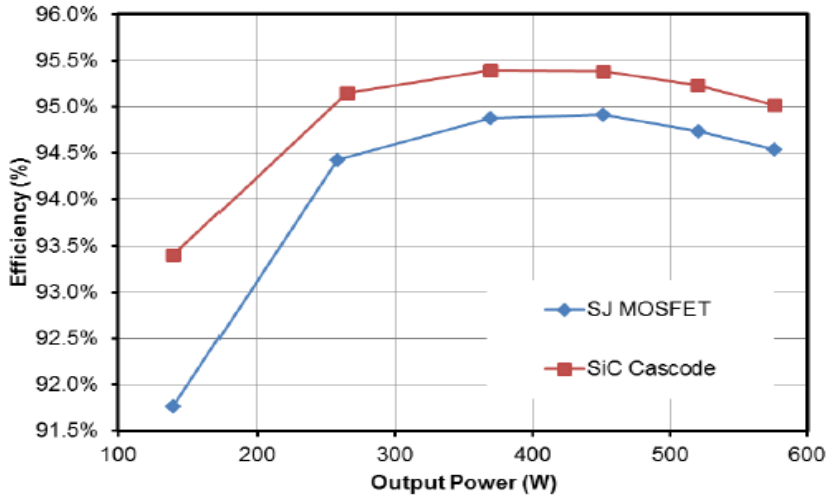




GeneSiC SEMICONDUCTOR

A 650V SiC Cascode Approach

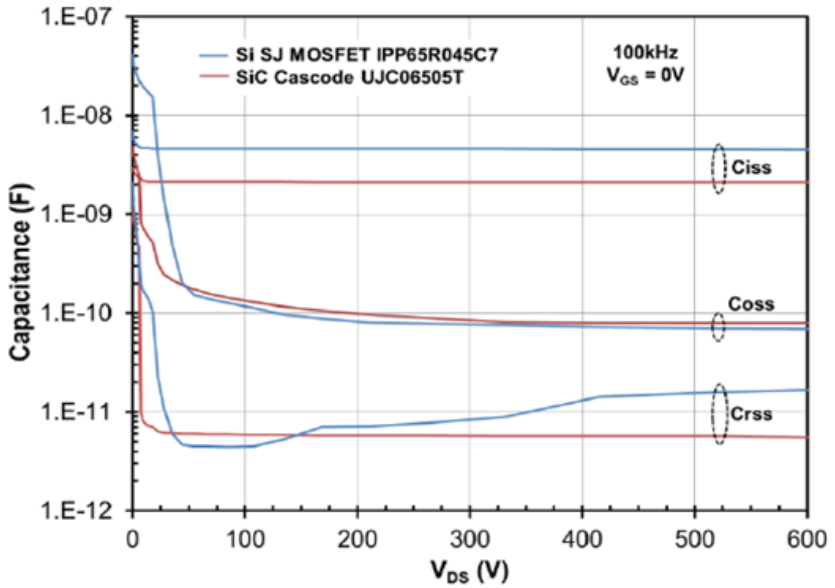
- "Ultra-low RdsA of 0.75mohm-cm^2 compared to 10mohm-cm^2 for Si SJ leads to 7.3X smaller die"
- "The die cost of the 6inch SiC solution will reach parity with Silicon"
- "Lower Rds*Qg, Rds*Eoss, excellent body diode recovery, adequate avalanche capability is compelling for high power applications"



Efficiency vs. output power for phase shifted full bridge with SiC cascode and Si superjunction MOSFET, 400V in, 24V out, f=75kHz

KEY DATASHEET PARAMETERS OF USCI'S 650V CASCODE SWITCH COMPARED TO SUPERJUNCTION MOSFET

Device	R_{DS}	Q_G	Q_{GS}	Q_{GD}	Q_{rr}	E_{OSS}	V_{TH}	TCR	Gate Drive	Die Area
	mΩ	*nC*	*nC*	*nC*	*μC*	*μJ*	*V*	*@ 150C*		
SiC Cacode UJC06505T	34	58	15	15	0.15	8	5	1.8	0 to 12V	1
Si Superjunction IPP65R045C7	40	93	23	30	13	11.7	3.5	2.4	0 to 12V	7.3×

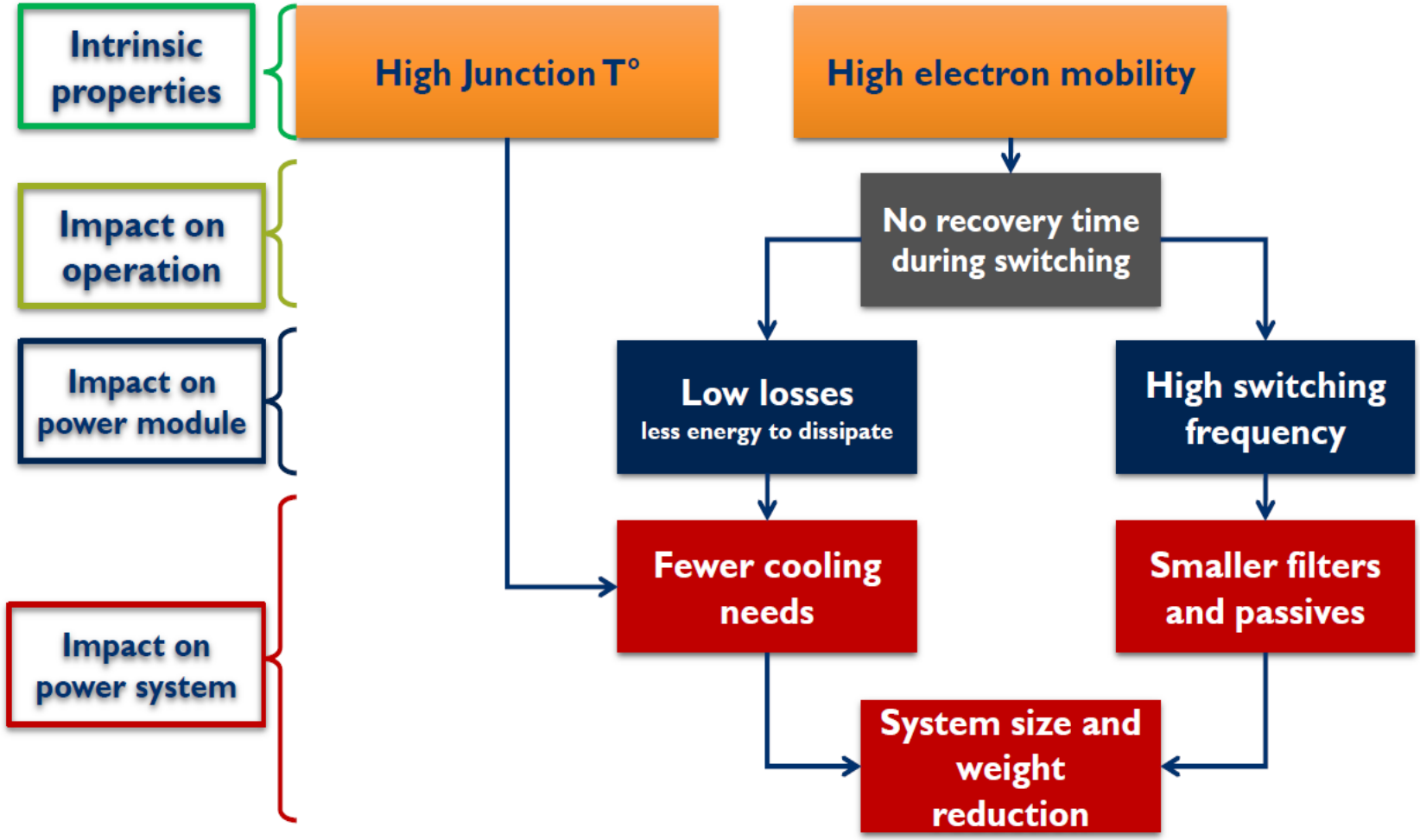


Capacitance curves comparison between SiC Cascode UJC06505T and superjunction MOSFET IPP65R045C7

WBG Enables Small Size, Low Weight

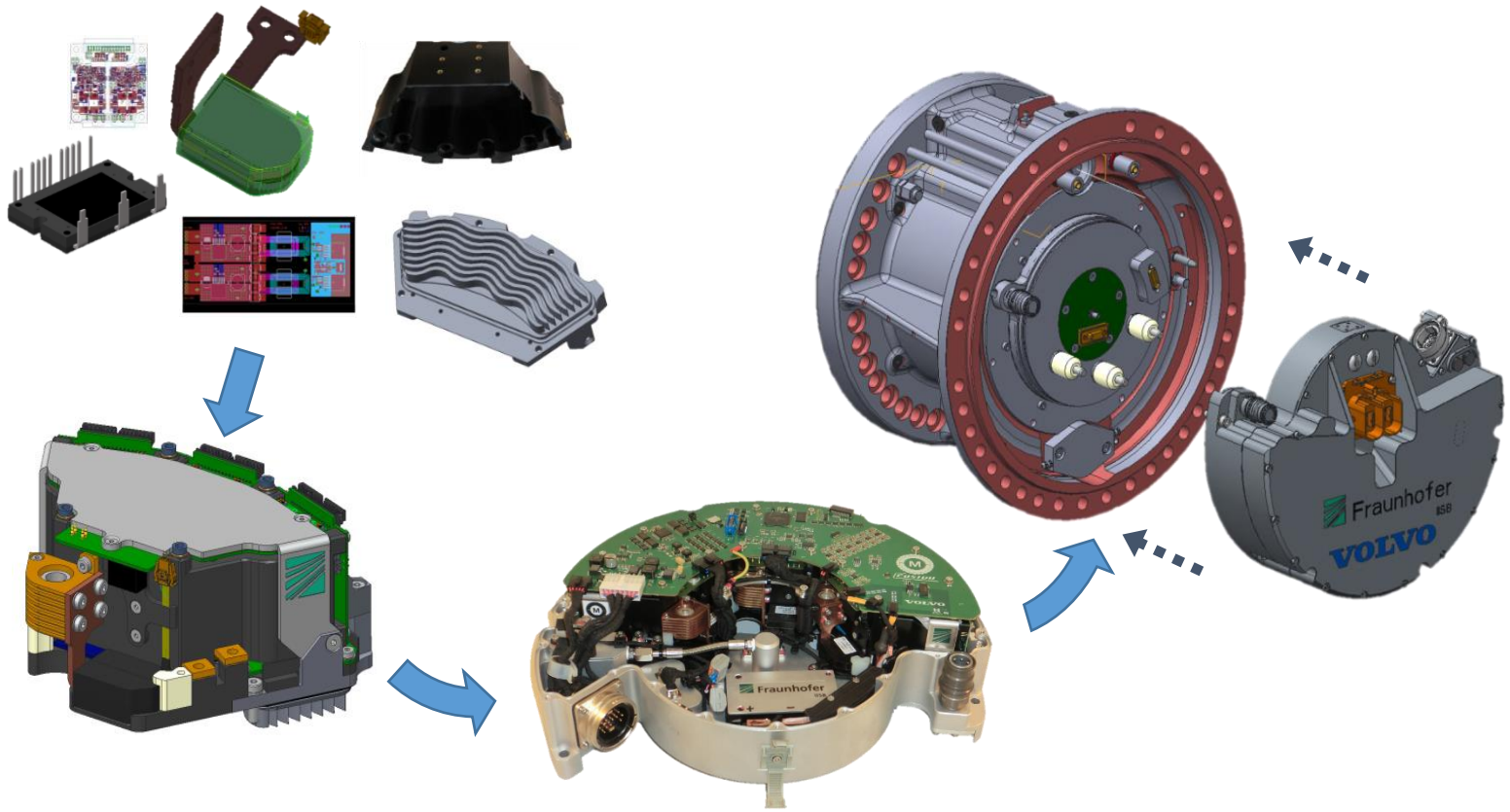
WBG means:

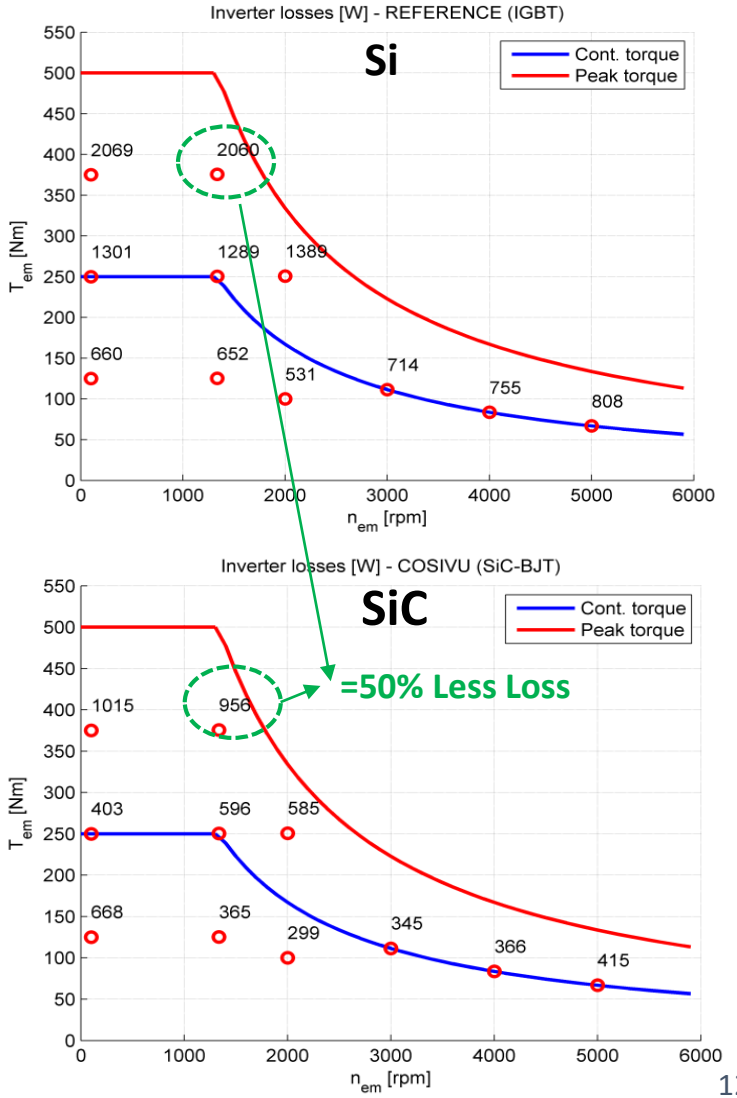
High Electric Field
Reduced Dimensions
Reduced Chip Size
Low Input Capacitance
Low Output Capacitance
Low Conduction Loss
Low Junction Leakage
High Thermal Conductivity
High Efficiency
High Power Density



Reference Yole, Toyota: Carele Tokyo, Jan'16:
http://www.slideshare.net/Yole_Developpement/what-does-the-future-of-automotive-market-hold-2016-presentation-yole-developpement-at-carele-japan-tokyo

EV Drive: 50% Less Loss Across Torque Range

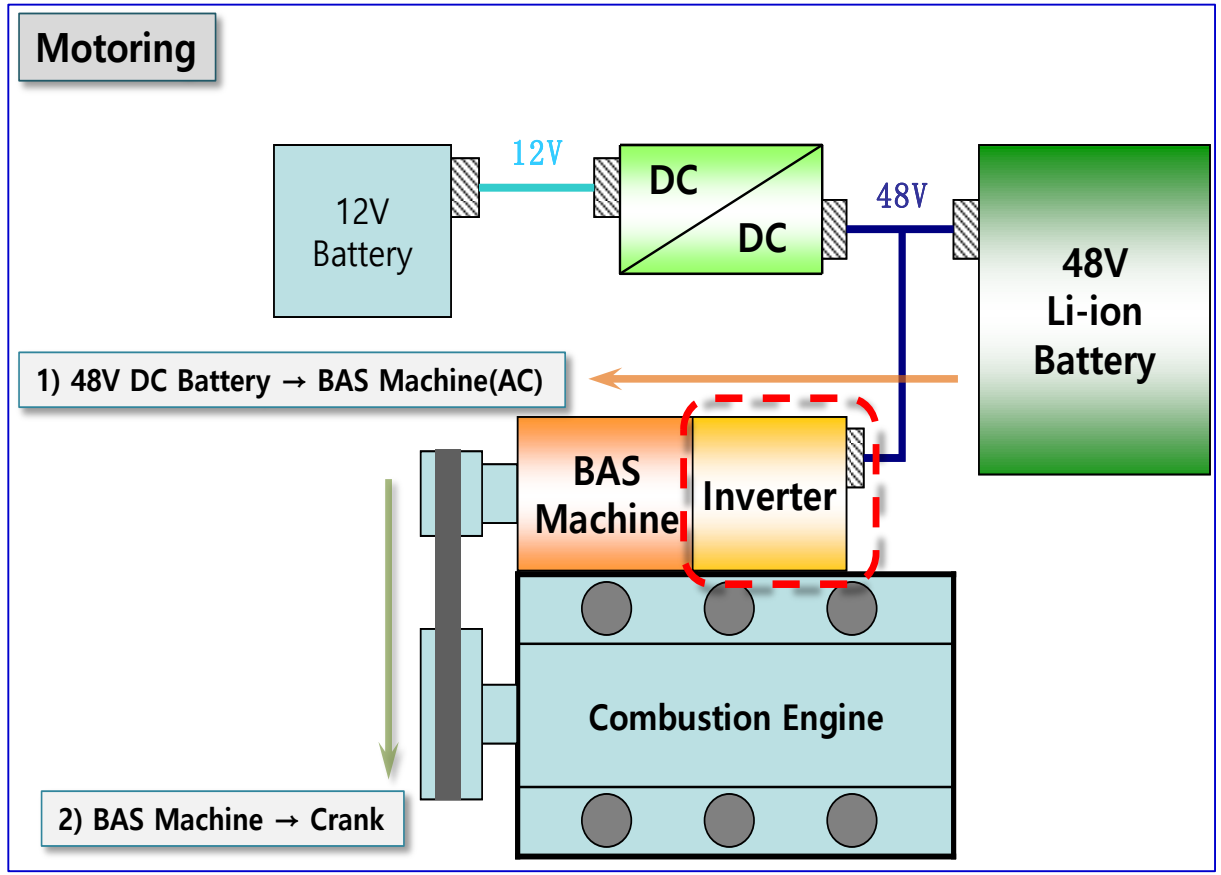




swerea IVF · VOLVO · TranSiC · NANOTEST Berliner Nanotest und Design GmbH · SENSITEC · FAIRCHILD · Fraunhofer ENAS · Fraunhofer IISB · HELLA · elaphe · TECHNISCHE UNIVERSITÄT CHEMNITZ

Courtesy of COSIVU Consortium 2015. See: http://www.cosivu.eu/template.asp?meny=67&lank=116

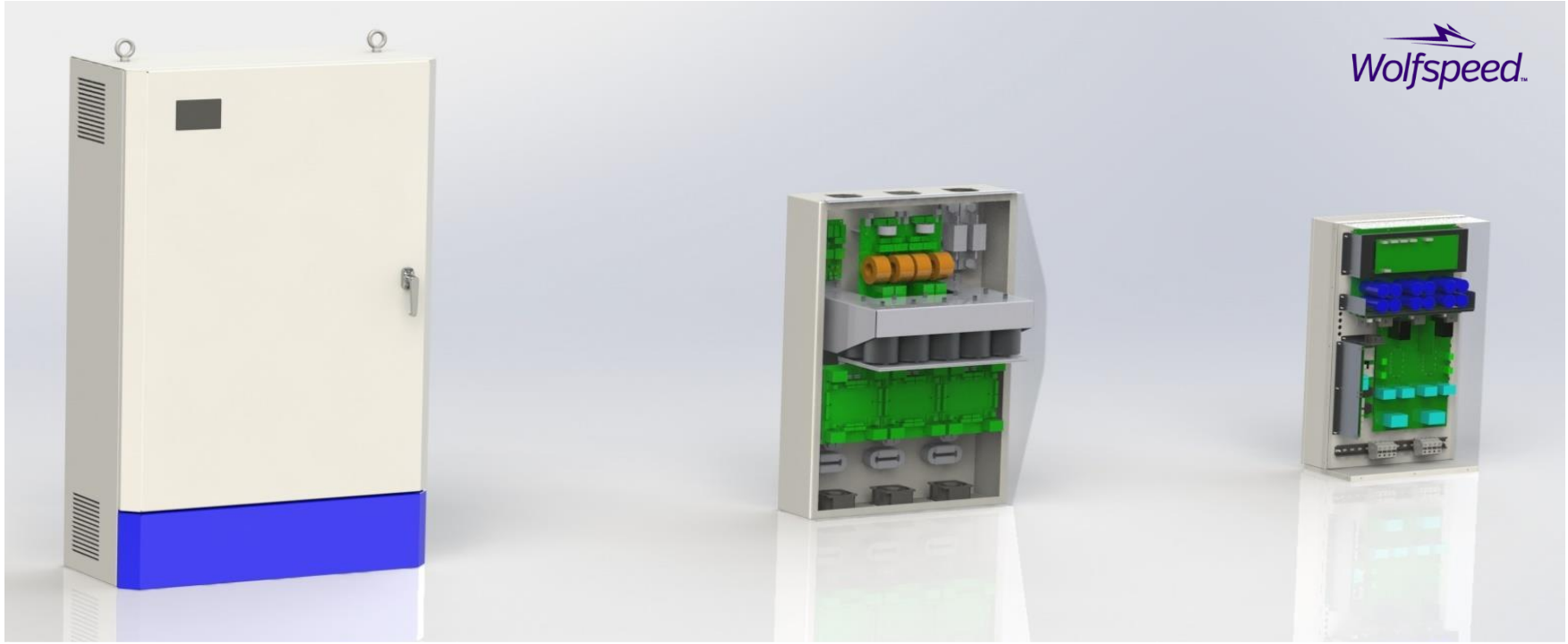
Mild Hybrid – 80% Smaller with 100V GaN



- 48V bi-directional inverter
- 12kW (motor drive) / 10kW (generating)
- 80% smaller
- 70% lighter
- +12% efficiency

Courtesy of GaN Systems

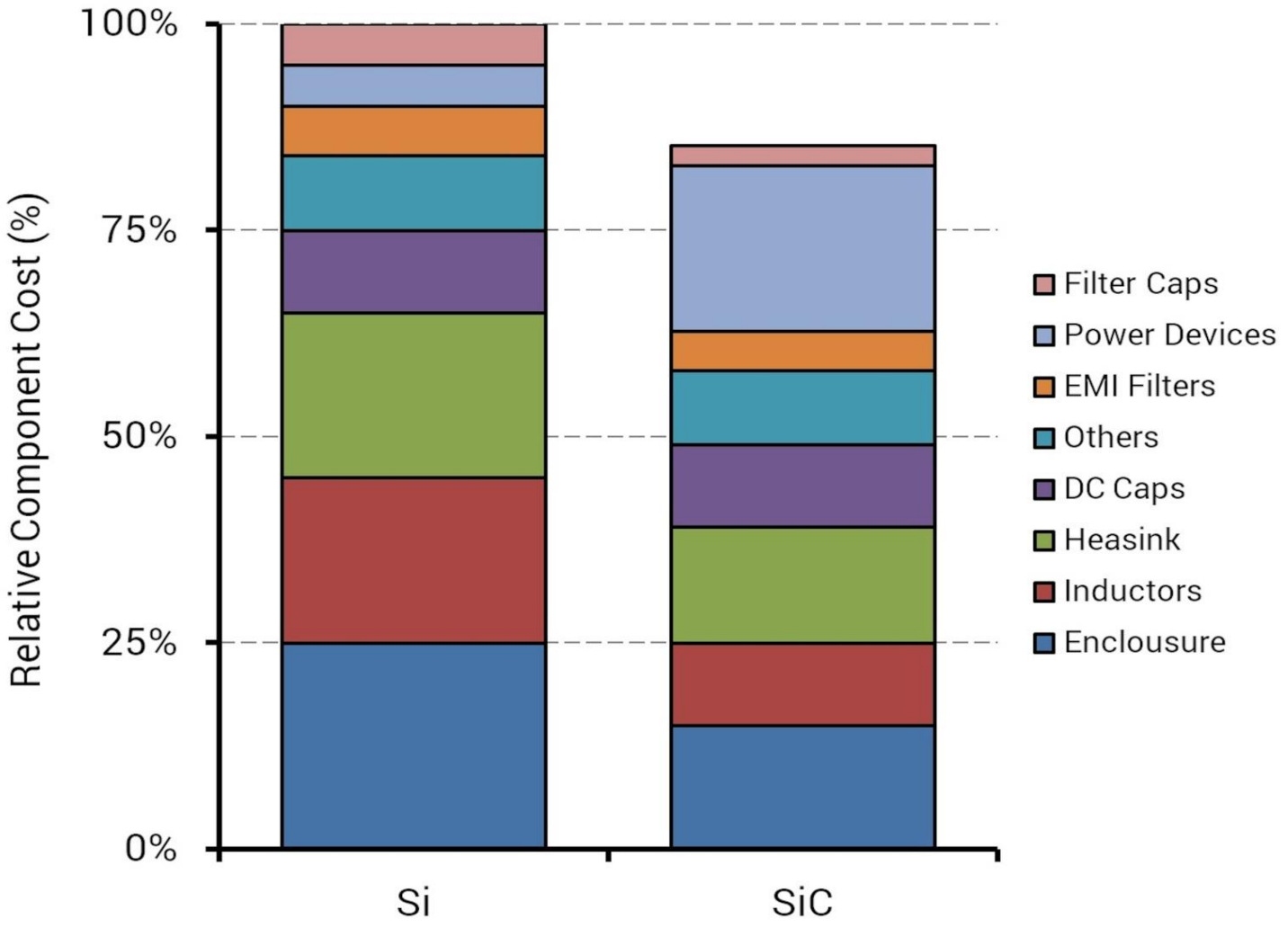
50kW Inverter: 75% Smaller, 80% Lighter with SiC



Year	2013		2014	2015
Powertrain	Si Module		SiC Discrete	SiC Module
Efficiency (peak)	98.3%	50% less loss		99.1%
Size (m^3)	0.41	50%-75% smaller	0.21	0.09
Weight (kg)	173	70%-80% lighter	50	33

Courtesy of Wolfspeed. Ref: http://www.electronicproducts.com/Power_Products/Invertors/The_impact_of_SiC_on_PV_power_economics.aspx

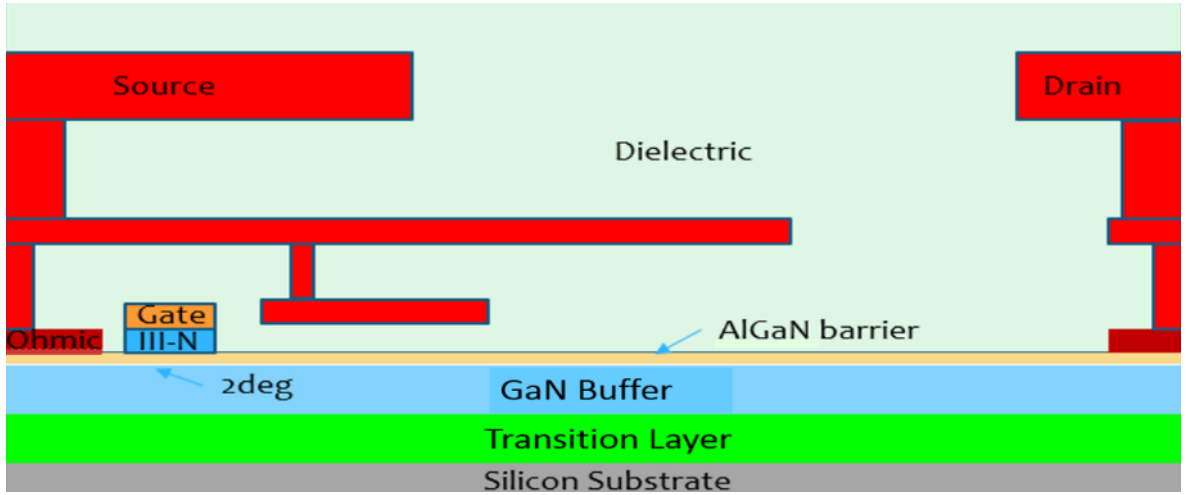
50kW Inverter: 15% Lower Cost with SiC

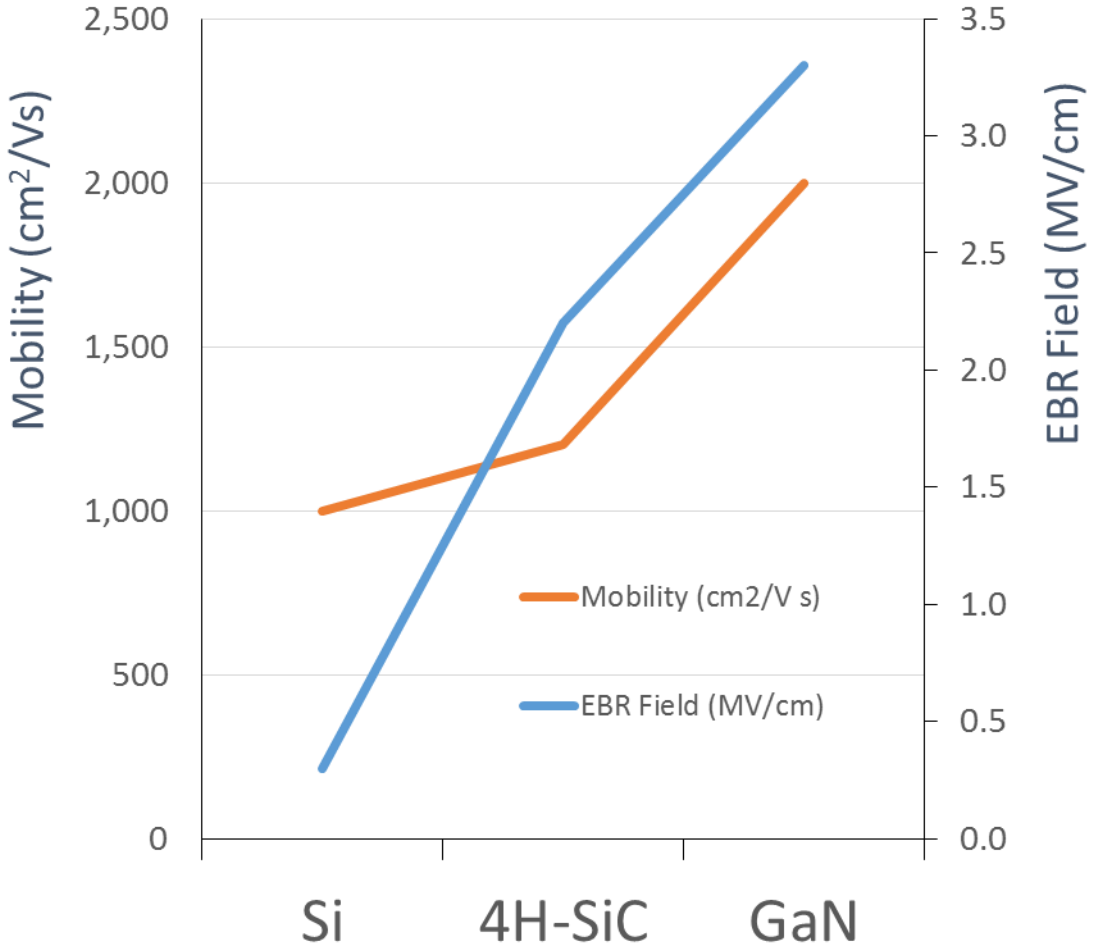


Courtesy of Wolfspeed

Lateral GaN Advantage for Off-line Applications

- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low Q_g and Q_{OSS} and allows integration
- Integration on silicon substrates means mature low cost wafer fabrication is available

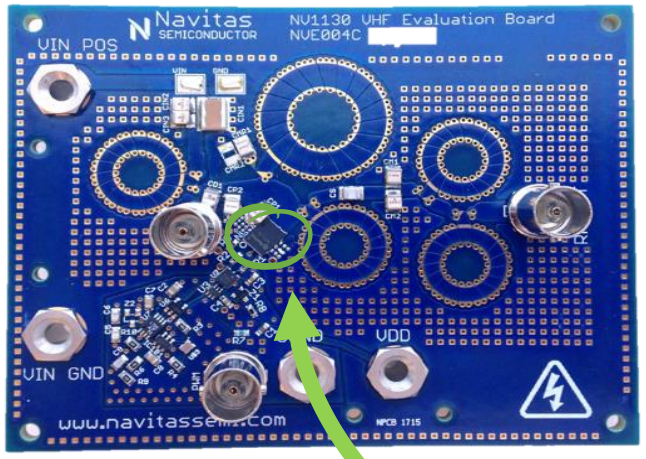


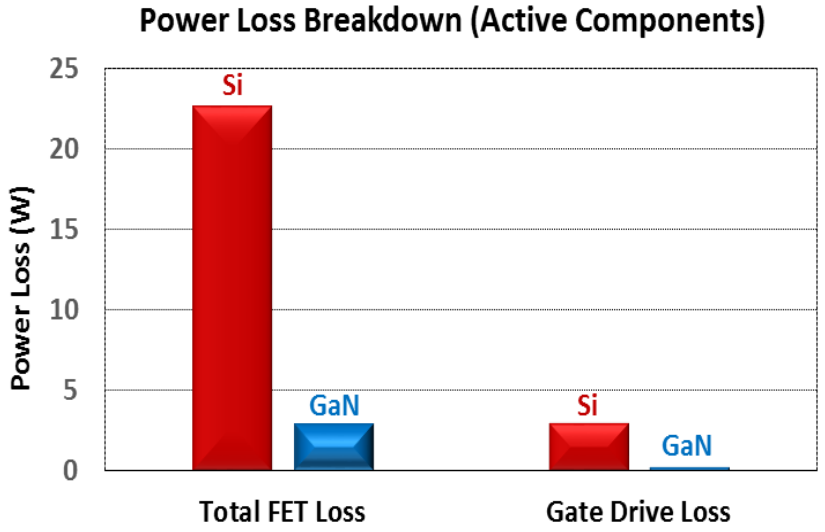


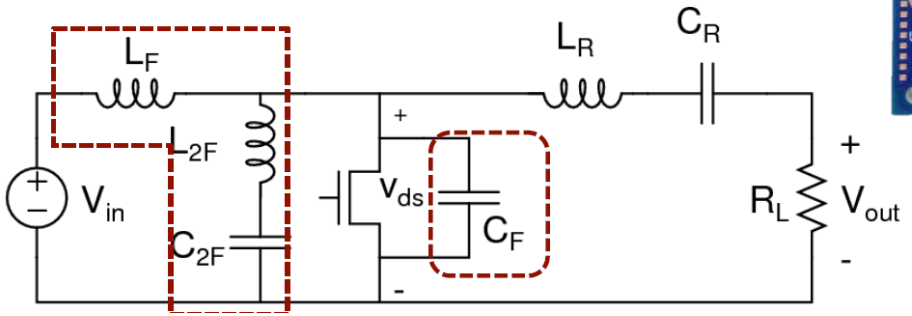
650V Navitas eMode GaN at 27MHz & 40MHz

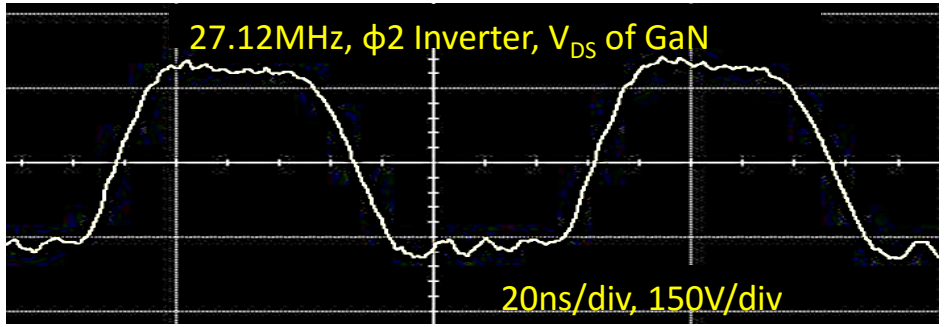
Class Phi-2 DC/AC converter: Stanford / Navitas demo

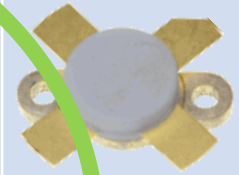
- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss



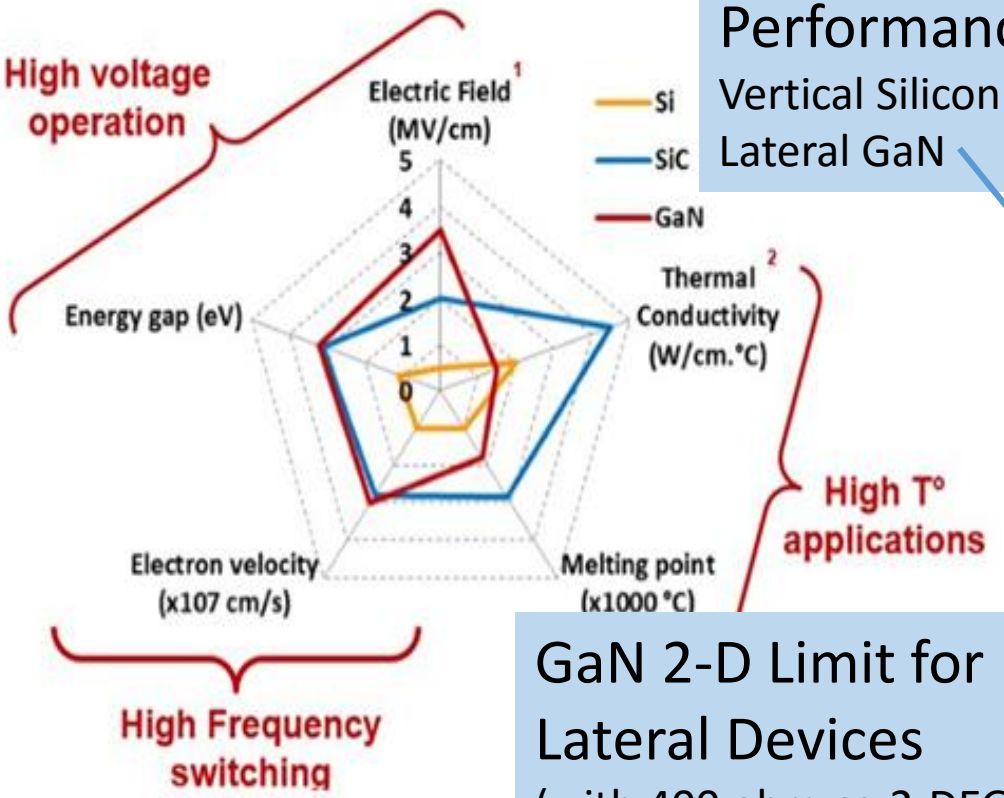






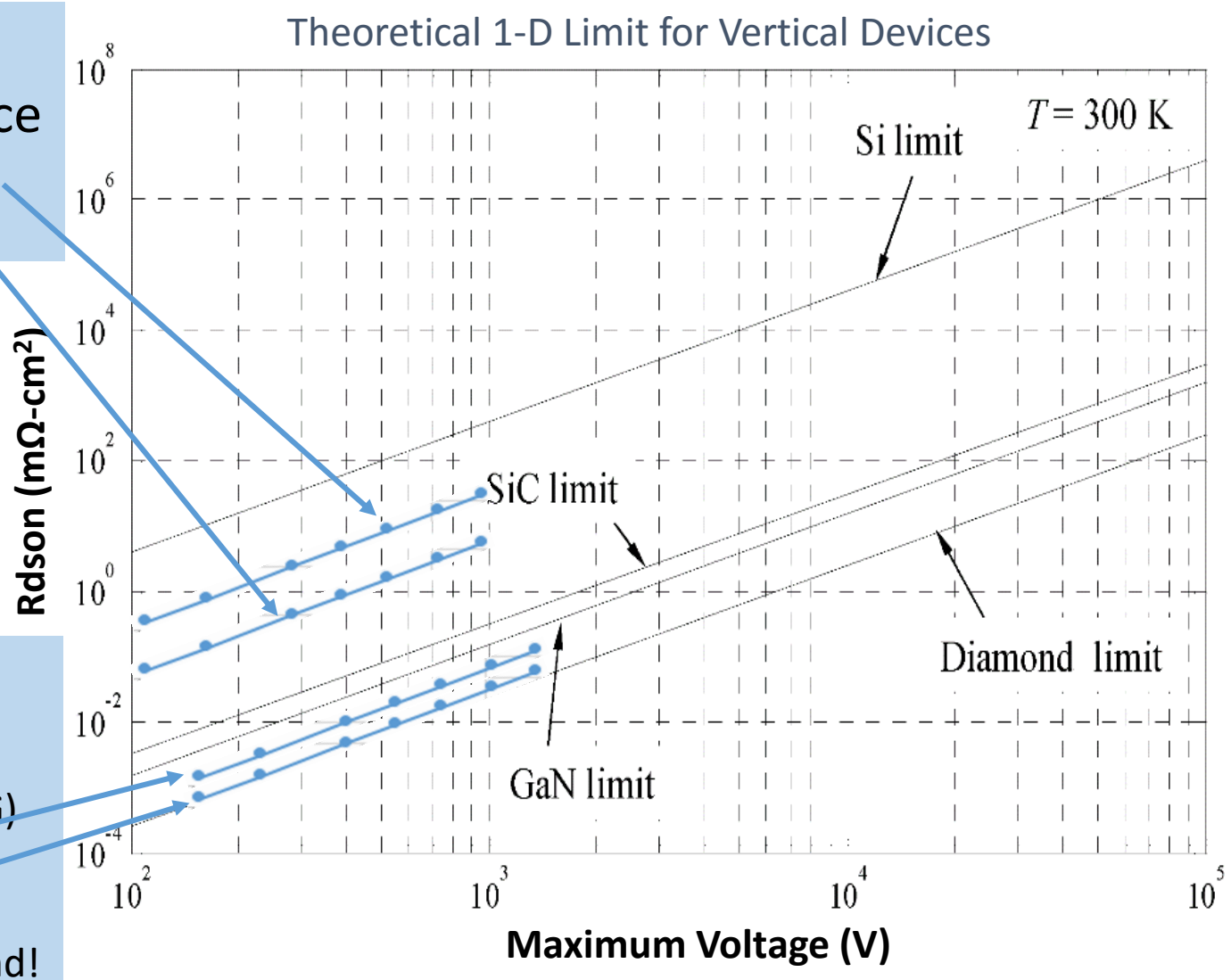
Technology	V	Pack (mm)		F_{SW} (MHz)	Eff. (%)	Power (W)
RF Si (ARF521) Microsemi POWER PRODUCTS GROUP	500	M174 22x22		27.12	91%	150
eMode GaN Navitas	650	QFN 5x6		27.12	96%	150
				40.00	93%	115

Performance Limits of WBG Materials



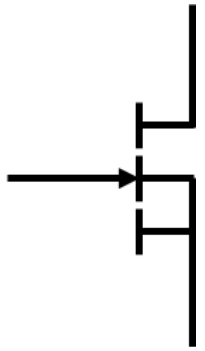
Current Performance
Vertical Silicon
Lateral GaN

GaN 2-D Limit for Lateral Devices
(with 400 ohm-sq 2-DEG)
2.5MV/cm
3.5MV/cm
Almost matches Diamond!



Creating the World's First AllGaN™ Power ICs

Fastest, most efficient
GaN Power FETs



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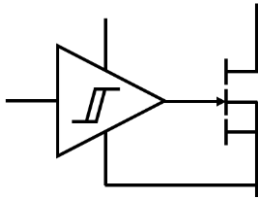
First & Fastest
Integrated GaN Gate Driver



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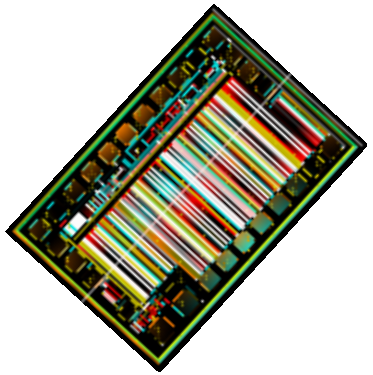
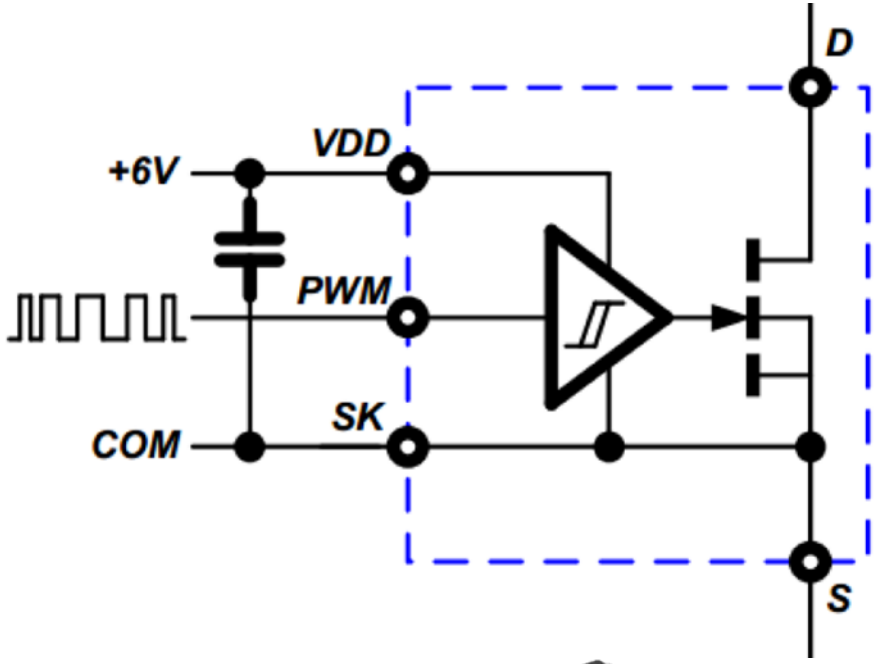
World's First
AllGaN™ Power IC

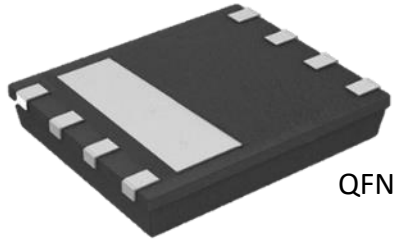


Up to 40MHz switching, 4x higher density & 20% lower system cost

Navitas GaN Power IC

- **Monolithic** integration
- 20x lower drive loss than silicon
- Driver impedance matched to power device
- Shorter prop delay than silicon (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Layout insensitive
- Industry-standard 5x6mm PQFN
  - High volume, reliable, low cost
  - Low profile (0.85mm), low inductance (0.2nH), low thermal resistance (<2°C/W)

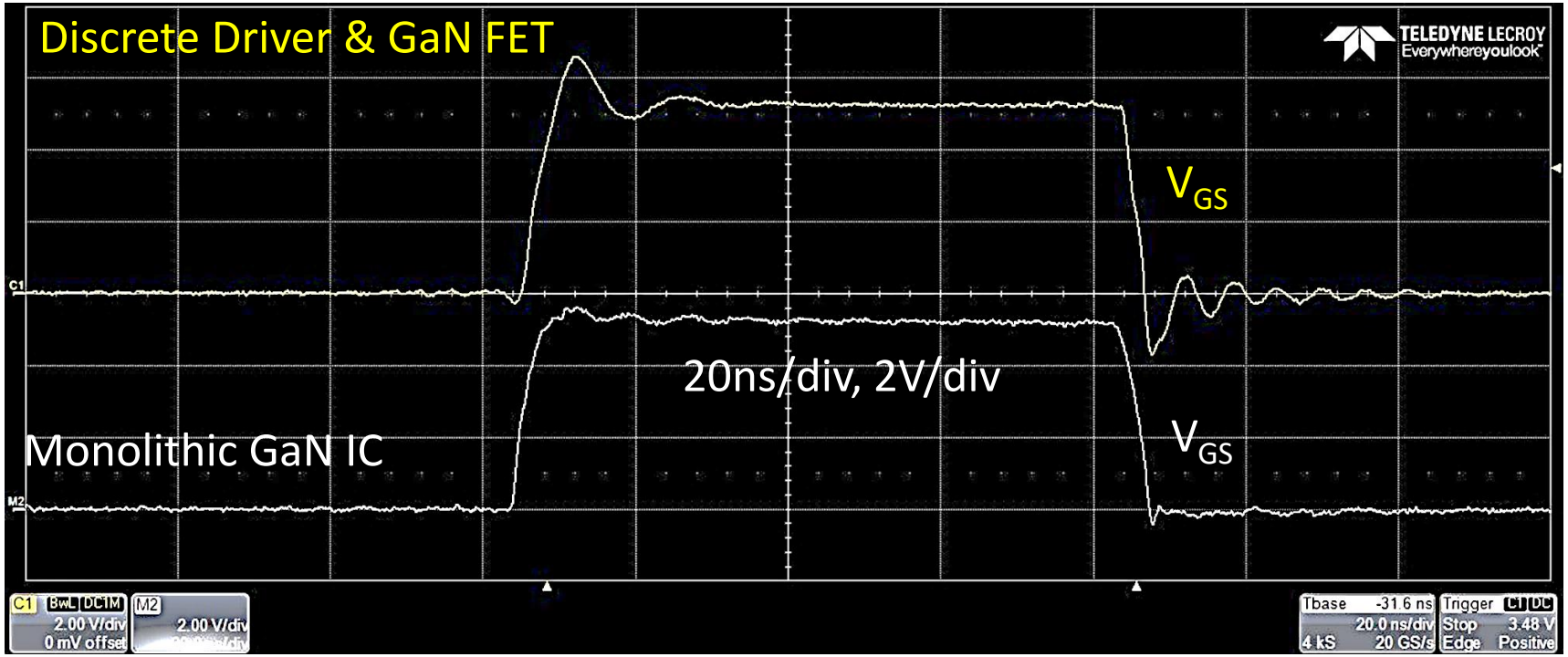




QFN 5x6mm

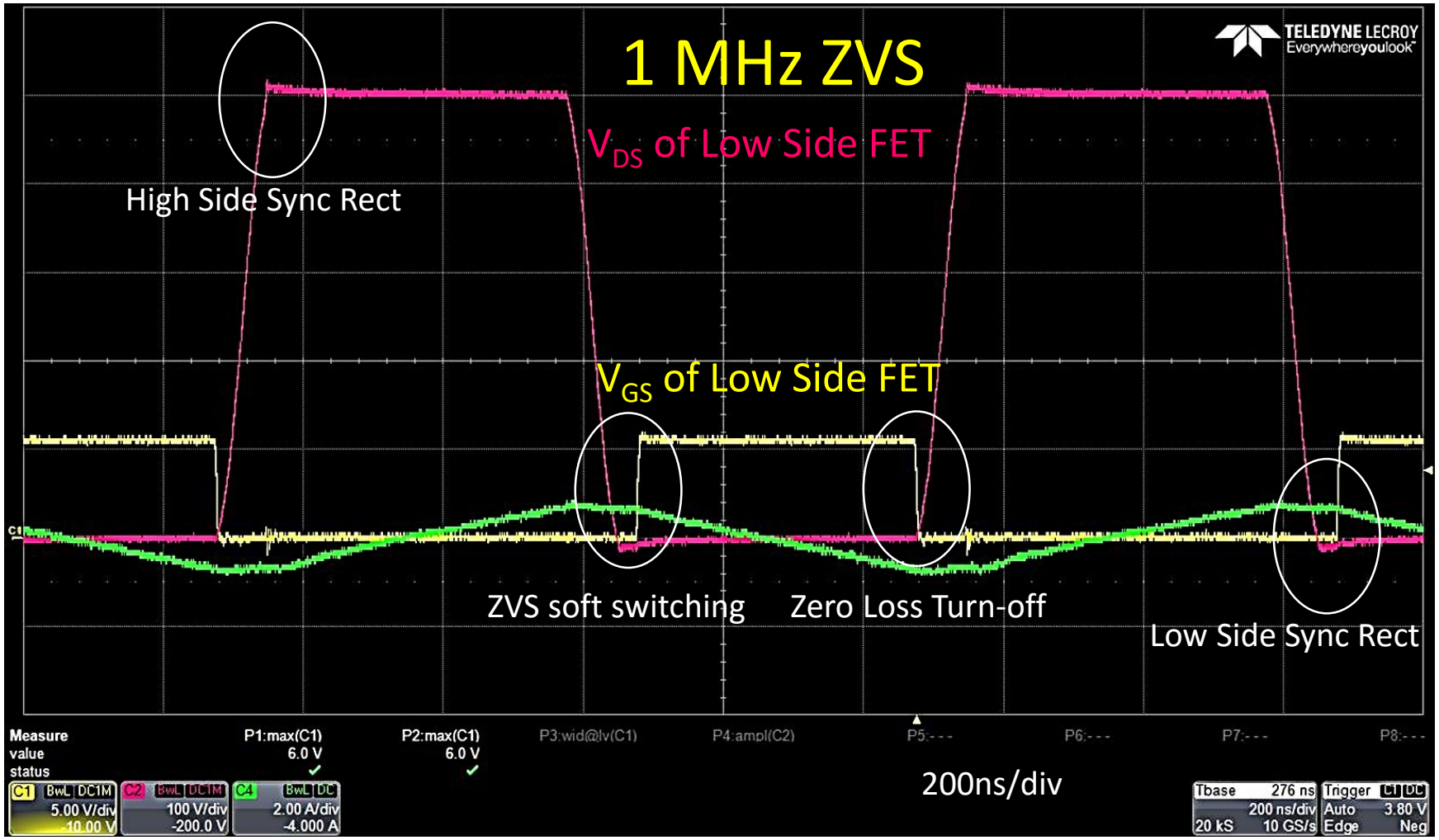
Crisp & Efficient Gate Control

- Monolithic Drive:
  - Eliminates gate overshoot and undershoot
  - Zero inductance on chip insures no turn-off loss



Smooth, clean, controlled waveforms

- 500V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- ZVS Turn-on
- Zero loss turn-off
- Sync rectification
- High frequency
- Small, low cost filter



Hard-Switch → Soft-Switch with GaN Power IC

Primary Switch Power Loss:

Minimized Minimized

$$P_{FET} = P_{COND} * k + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10x ~~2-3x~~ (GaN C_{OSS} charging/discharging loss negligible up to 2MHz)
- P_{DRIVER} ↓10x (GaN P_{DR} negligible up to 2MHz)
- P_{QRR} = 0
- P_{DIODE} ↓3x ~~2x~~ (synchronous rectification with improved dead-time control)
- $P_{T\text{-}OFF}$ = 0 ~~Reduced~~ (near-zero drive loop impedance with integration)

>10x frequency increase possible with higher efficiencies

The MHz Eco-System

- Navitas GaN Power ICs plus…
  - High-frequency controllers (PFC, PWM, DSP, LLC, SR)

  - High-frequency magnetics

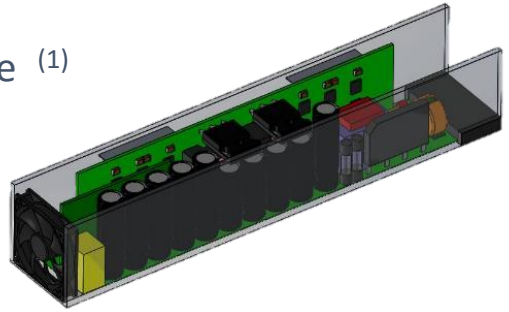
  - High-frequency SR FETs

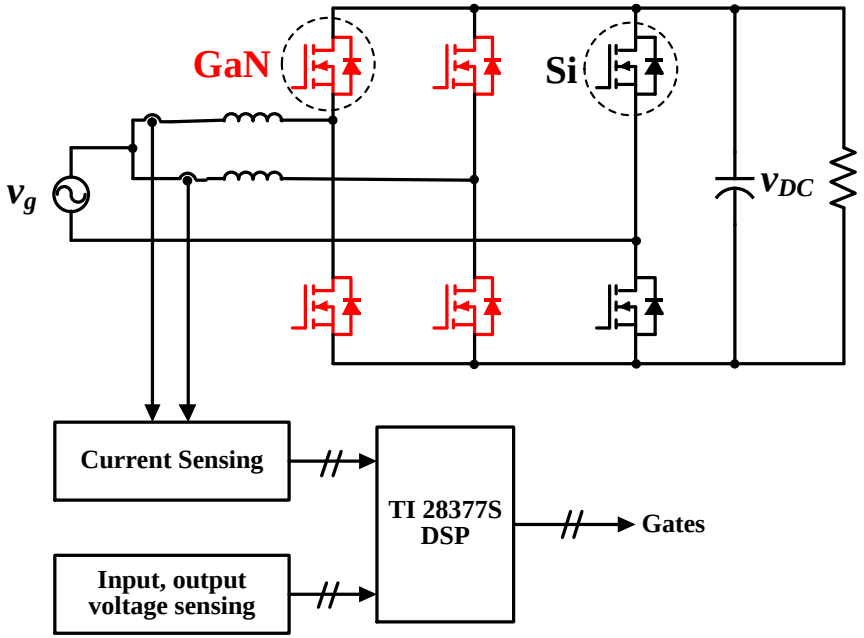
3kW PFC (2-phase Totem-Pole CrCM)

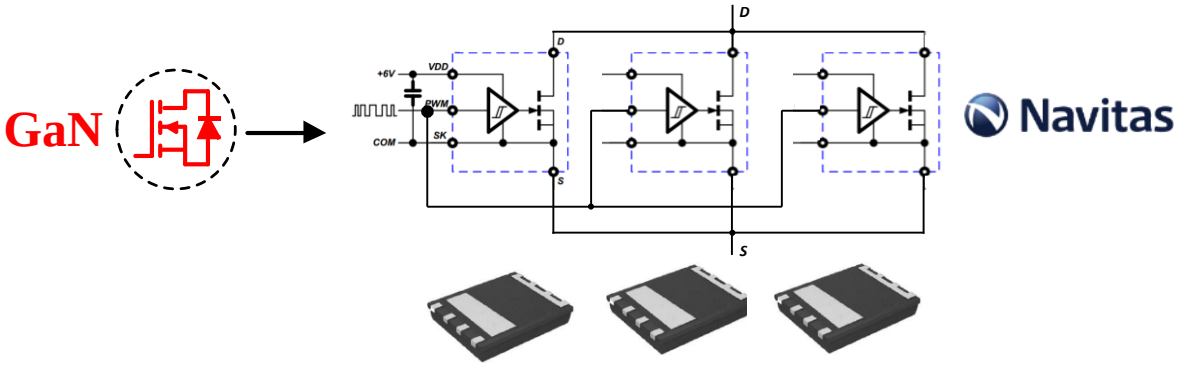
- Input : $220V_{AC}$ (47-63Hz)
- Output : 400V, 3,000W
- Frequency* : 1MHz each phase

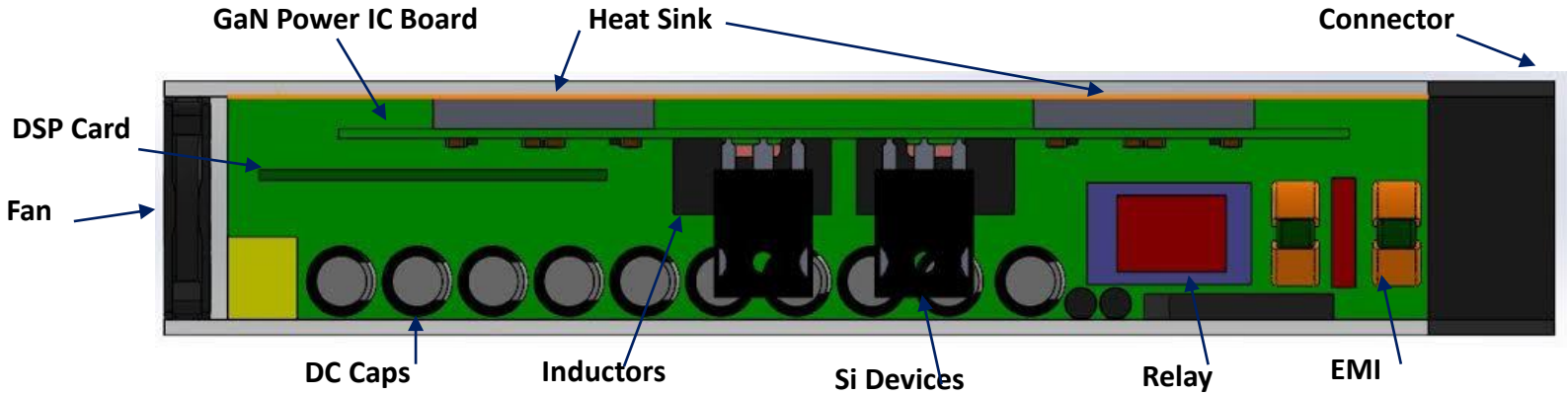
**Dual phase variable frequency interleaving (500kHz – 1.5MHz range)*

- Efficiency : >99% @ 800kHz, 200-1200W/phase (1)
  >98.8 @ 500kHz, 1800W /phase (1)
- Power Factor : >0.995 (1)
- Power Density : 135W/in^3 (2)
- Size : 220 x 35mm x 1U (2)







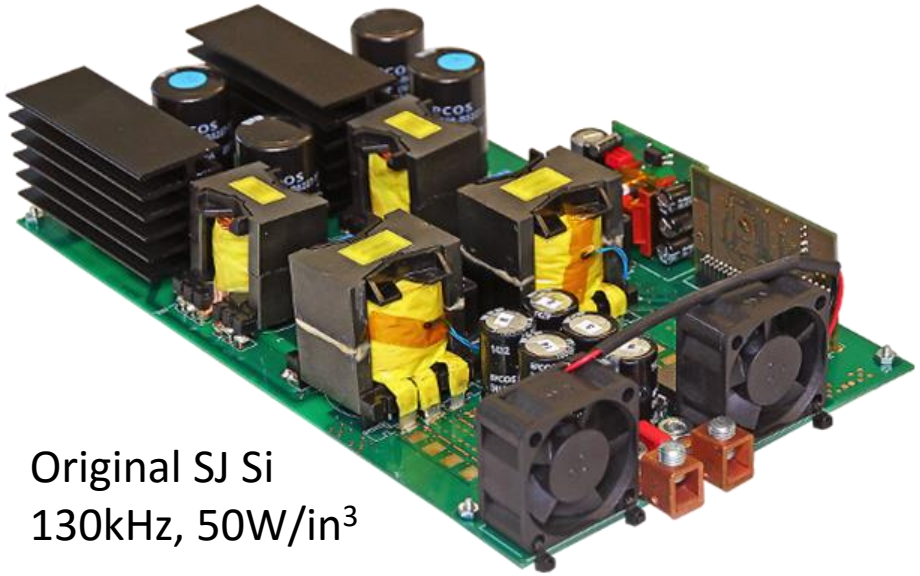


(1) Achieved on Alpha prototype
(2) Target for Beta prototype

3kW LLC: 2x–3x Smaller with GaN

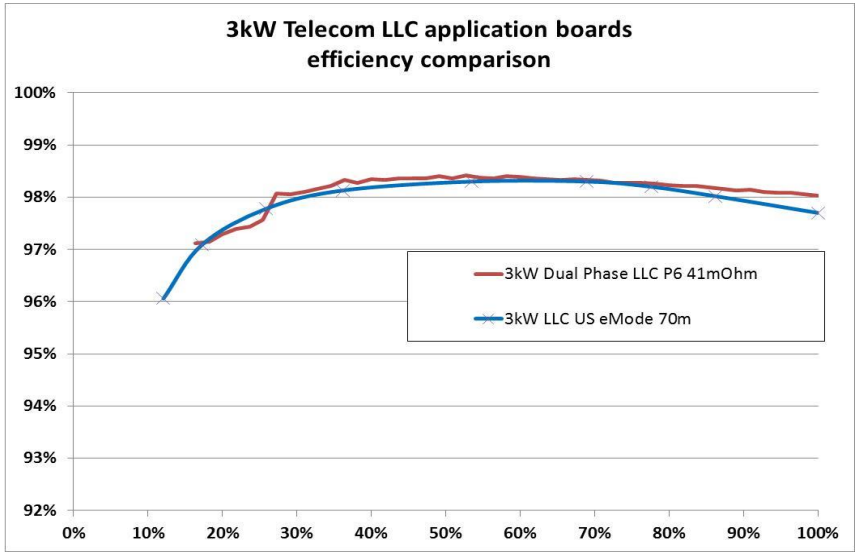
- Input : $380V_{DC}$
- Output : 52V, 3,000W
- Frequency : 350kHz

- Efficiency : 98.4% peak
- Power Density : $140W/in^3$ (2)
- Size : 152 x 91 x 32mm



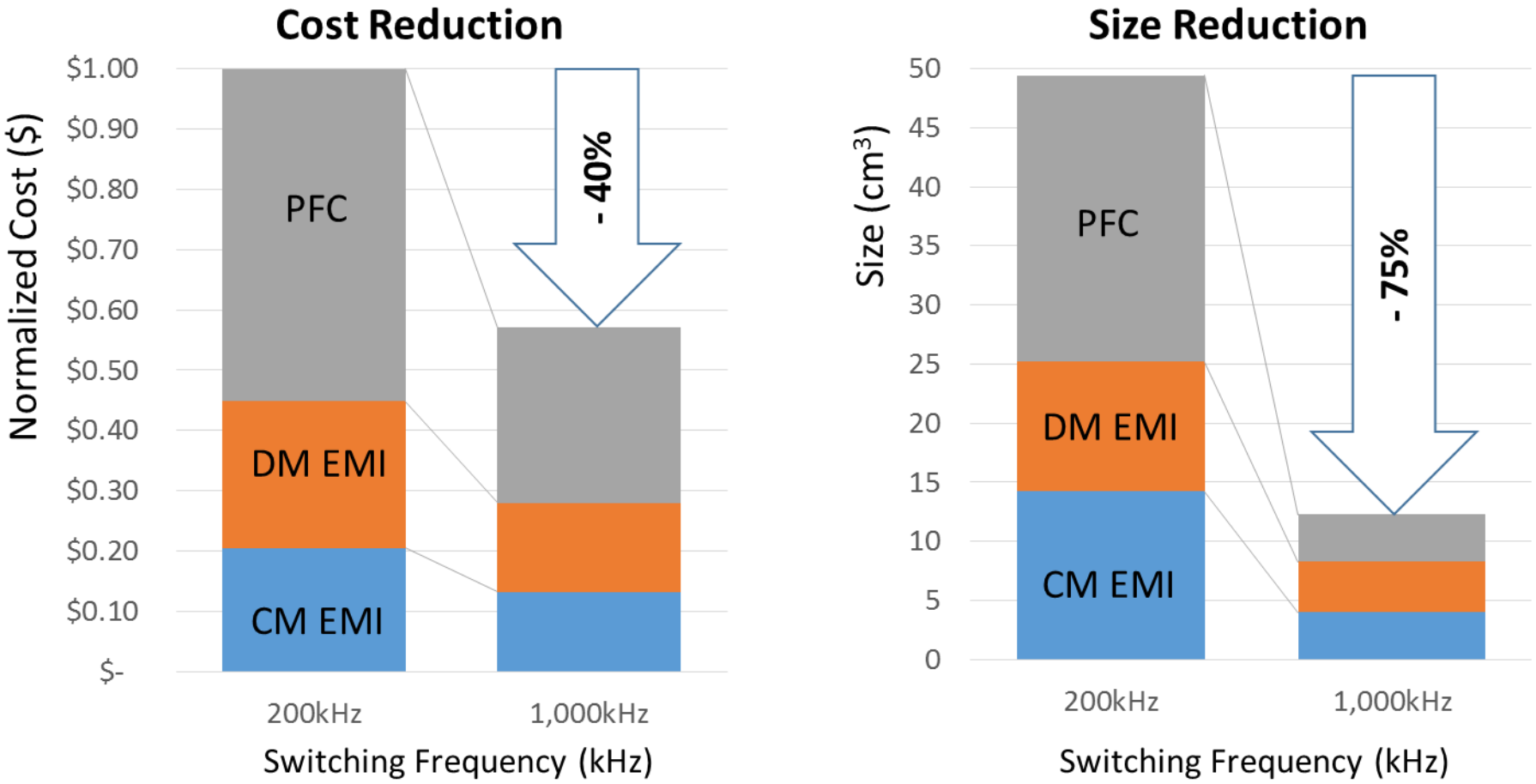
Original SJ Si
130kHz, $50W/in^3$

New CoolGaN™
350kHz, $140W/in^3$



Courtesy of Infineon

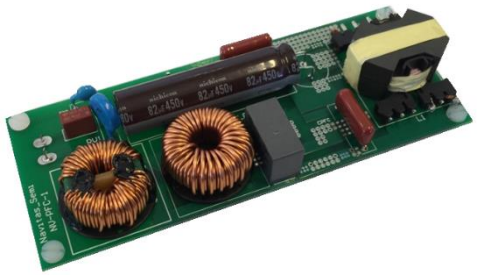
Higher Frequency = Smaller, Cheaper



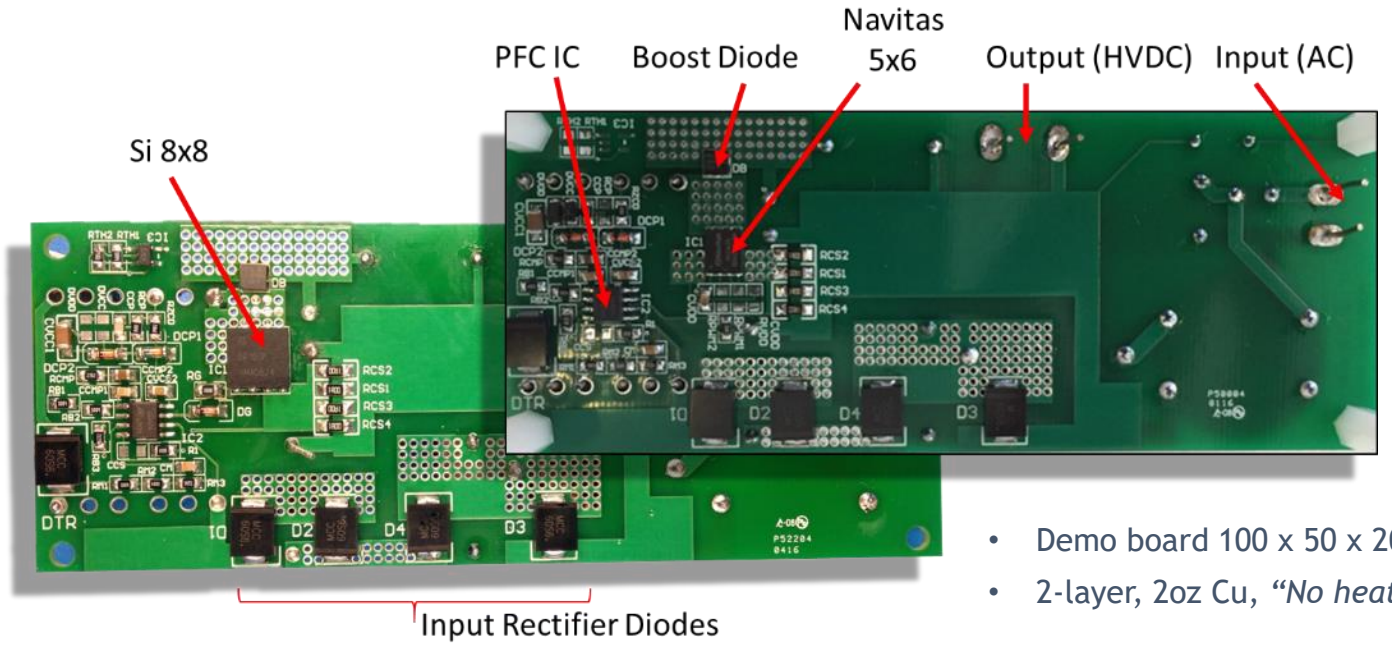
EMI & PFC Magnetics

SJ Si vs. GaN Power IC (CrCM PFC 150W)

	Pack	$R_{DS(ON)}$ mΩ	Q_G nC	$C_{OSS}(er)$ pF	$C_{OSS}(tr)$ pF	$R*Q_G$ mΩ.nC	$R*C_{OSS}(tr)$ mΩ.pF	$R*C_{OSS}(er)$ mΩ.pF
Navitas	5x6	160	2.5	30	50	400	8,000	4,800
IPL65R199CP	8x8	180	32	69	180	5,760	32,400	12,400
IPL60R130C7	8x8	115	35	53	579	4,025	66,600	6,100
GaN Benefits	**>50%**	**n/a**	**>10x**	**>2x**	**>10x**	**>10x**	**>7x**	**>2.5x**



- AC to 400V_{DC}, 150W
- 120V = 167-230kHz
- 220V = 230-500kHz
- 265V = 1MHz *(limited by PFC IC (L6562A)*

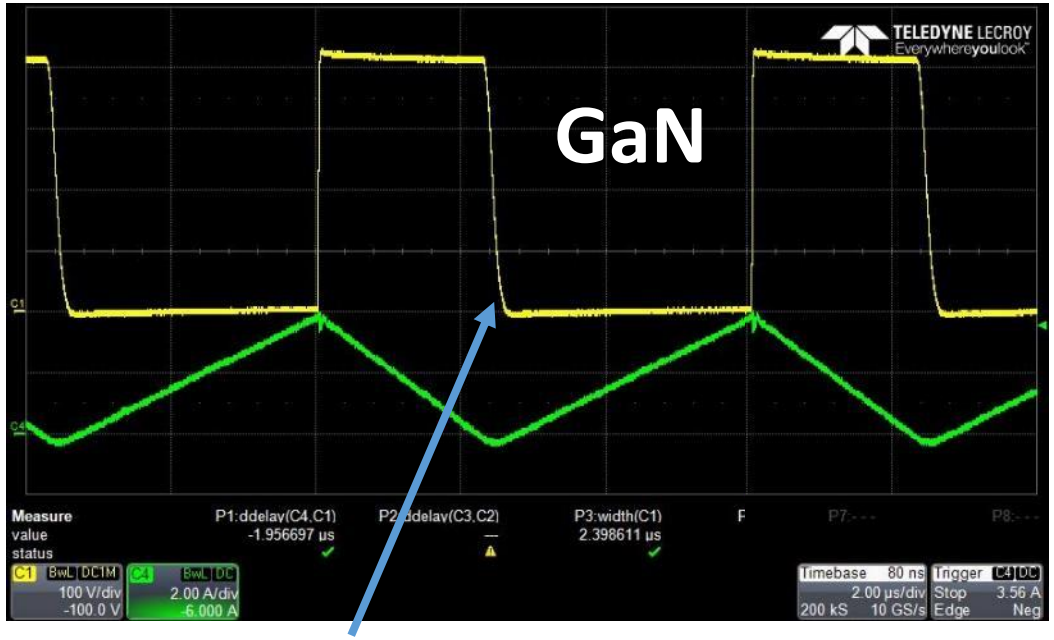


- Demo board 100 x 50 x 20mm
- 2-layer, 2oz Cu, *"No heatsink"* design

Si Starts Hard Switching as Frequency Increases

120V_{AC}, Si CP partial hard-switching (~200kHz)

- Voltage spikes
- Partial hard-switching (loss)



120V_{AC}, GaN clean ZVS waveforms (~200kHz)

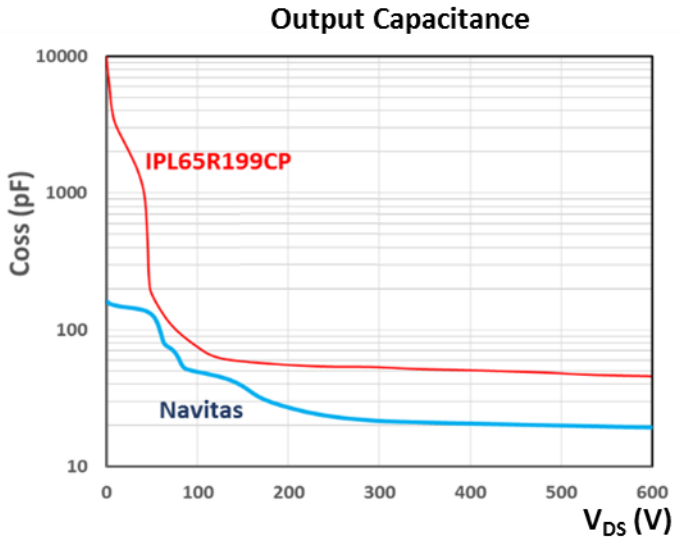
- No voltage spikes / overshoot
- Clean ZVS turn-on transition
- Minimize deadtime for low reverse conduction loss

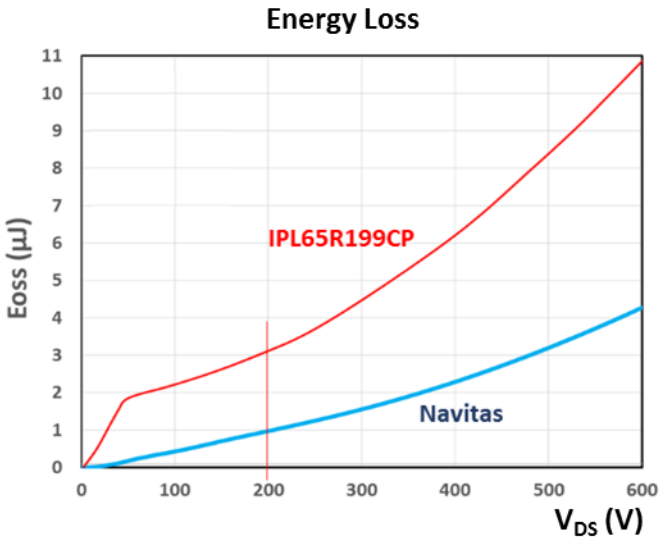
Si: High C_{OSS} = Long ZVS Transition = Trapped Energy

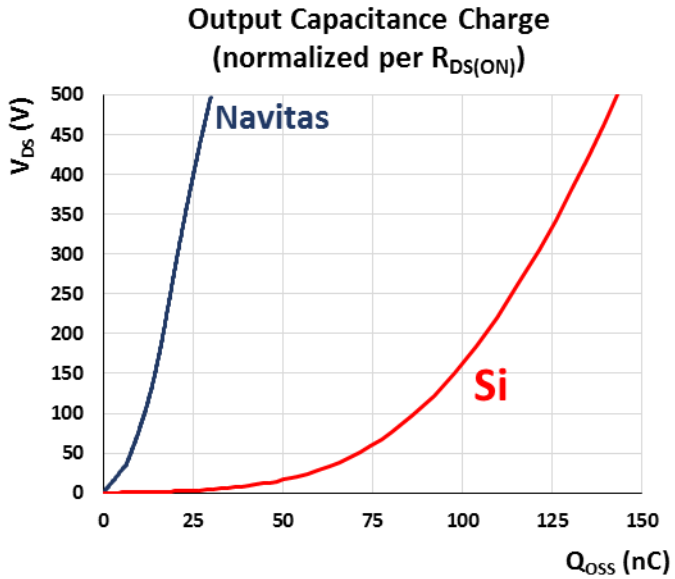
- Switching loss:
  $P_{LOSS} = E_{OSS}(V_{DS}) * F_{SW}$
- C_{OSS} → Delay (limits F_{SW})
- Too slow → partial ZVS → **E_{OSS} loss**

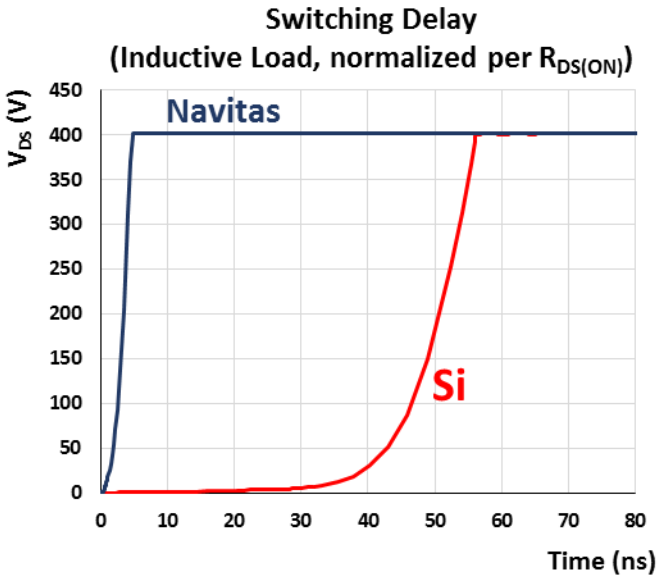
- Si C_{OSS} is 50x-100x higher than GaN at V_{DS} < 30V
- Si P_{LOSS} is 3x higher than GaN at 200V (partial ZVS)
- Big effect at full or light load condition

- Further information: "C_{OSS} Hysteresis in Advanced Superjunction MOSFETs", Harrison, APEC 2016

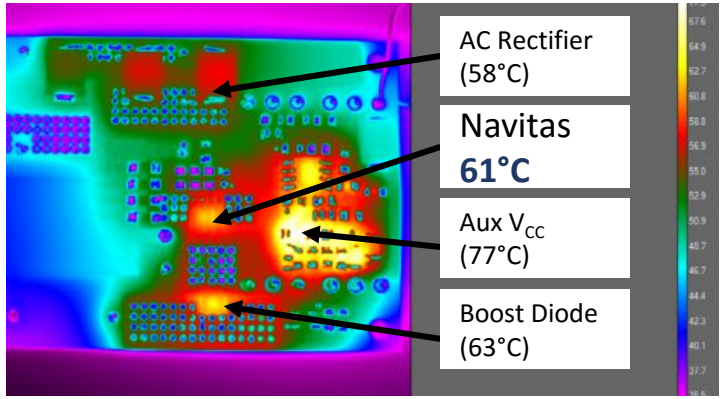




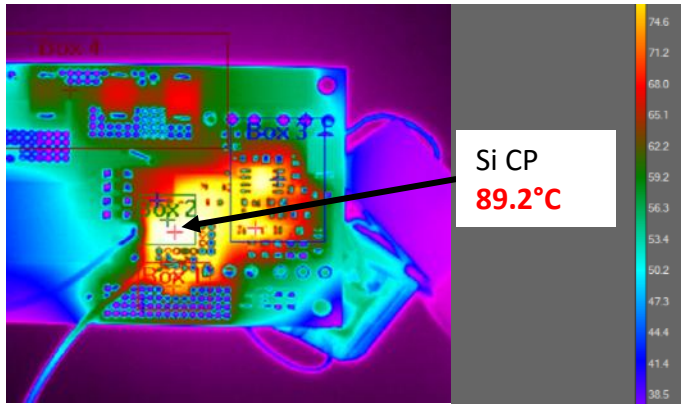




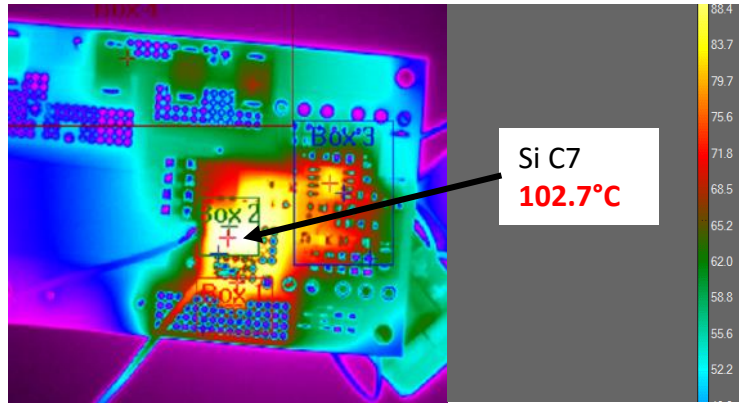
Full Load Performance



220V_{AC}, 150W



220V_{AC}, 150W



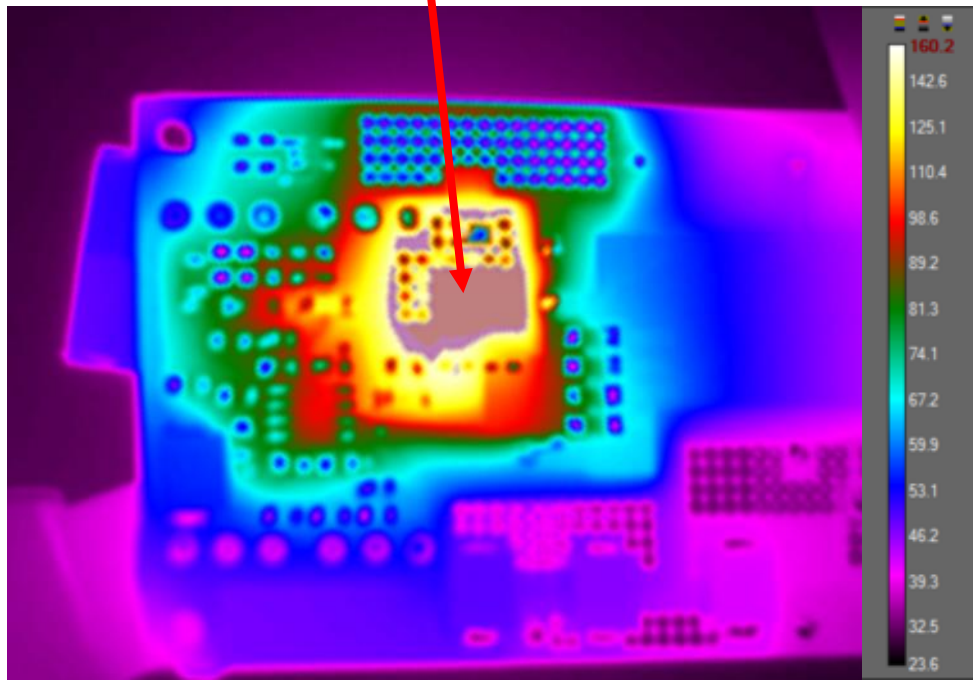
180V_{AC}, 150W

- GaN runs cool (61°C)

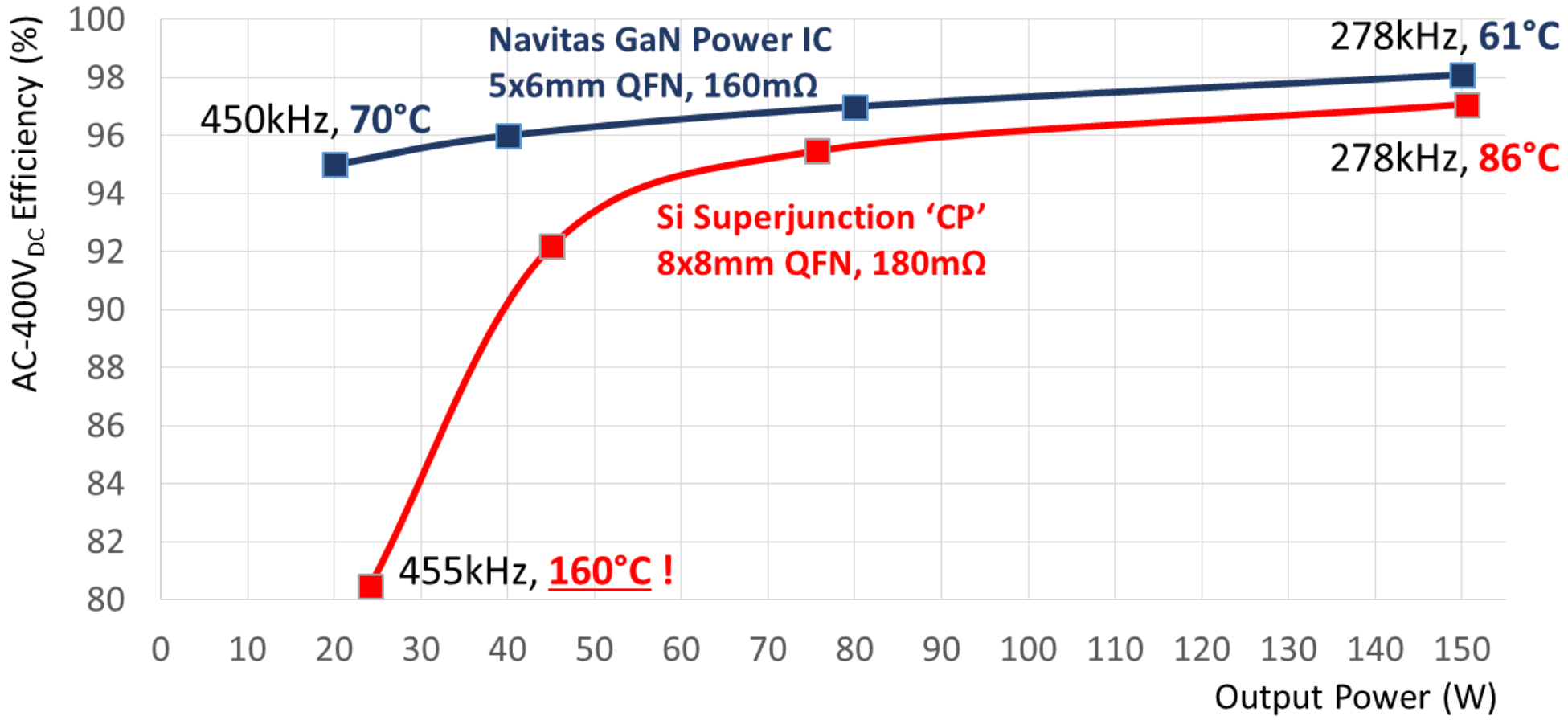
- CP Si running >90°C
- C7 Si too hot to run at 220V_{AC}

Light Load = High Frequency = High Loss for Si

Si switching loss: P_{LOSS} = E_{OSS} (V_{DS}) *frequency (at 20W)
= 3.5uJ * 455kHz
= 1.59W → = 160°C !

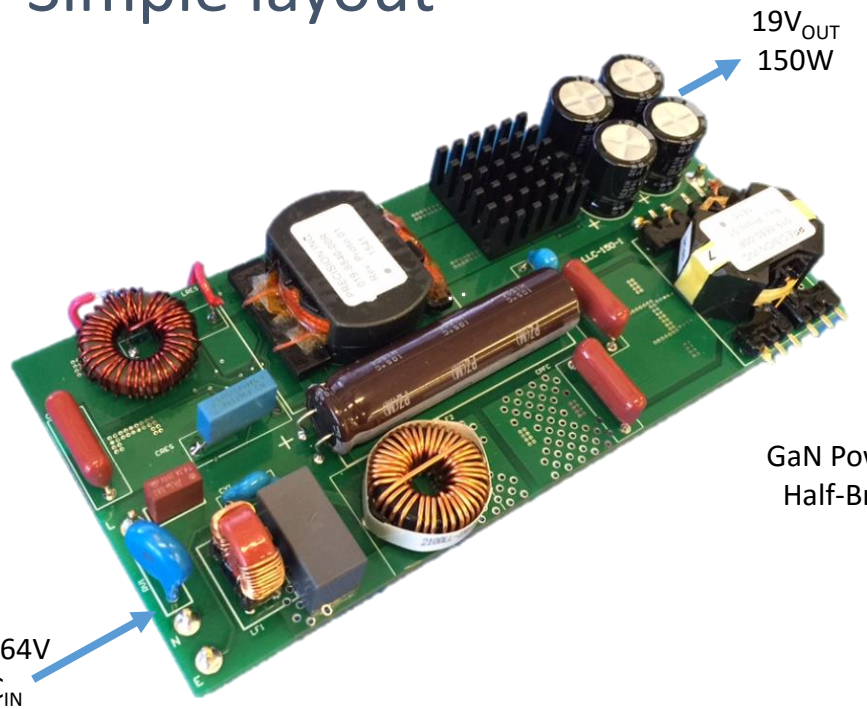


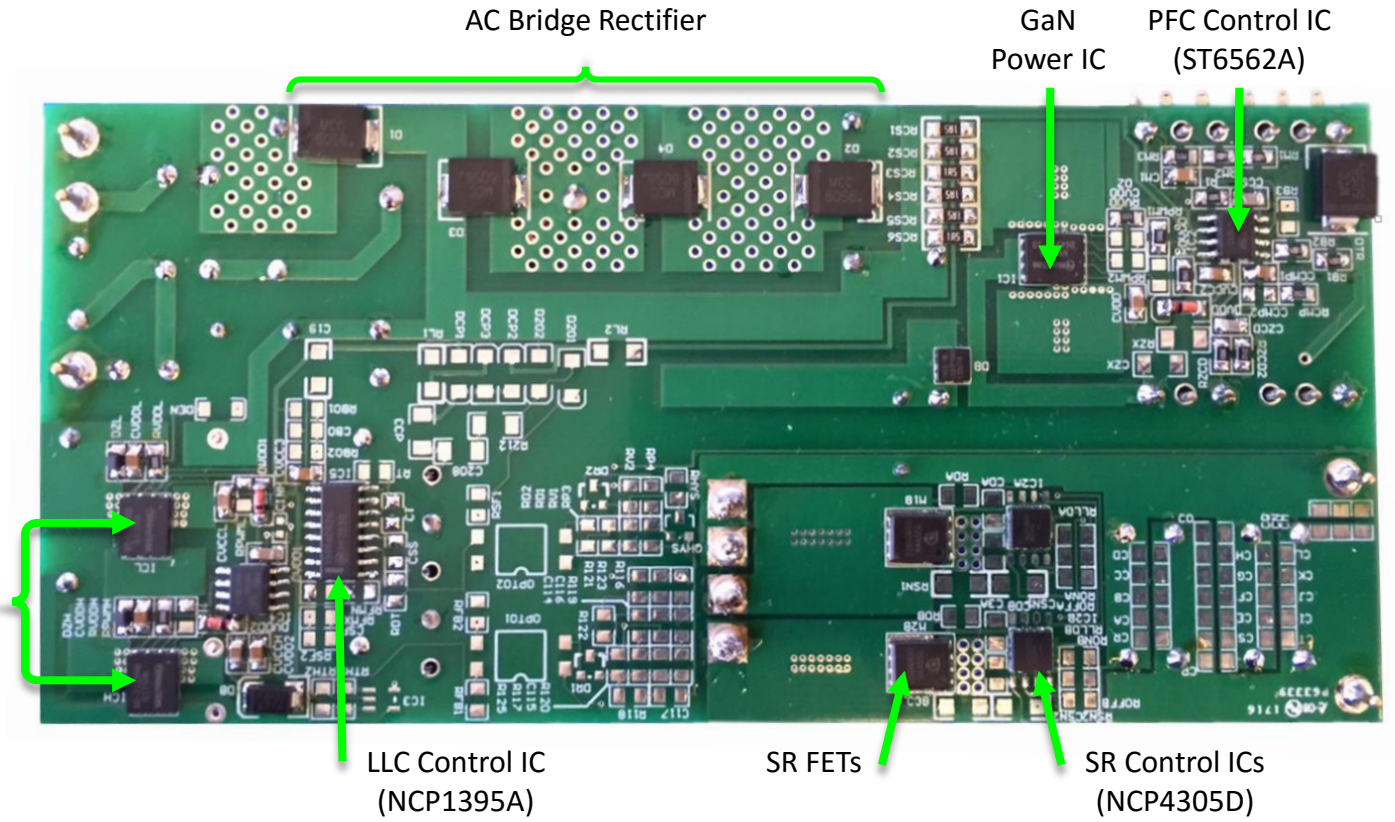
Hot Si, Cool GaN



AC-19V: GaN Power ICs in PFC, LLC

- Simple schematic
- Simple layout

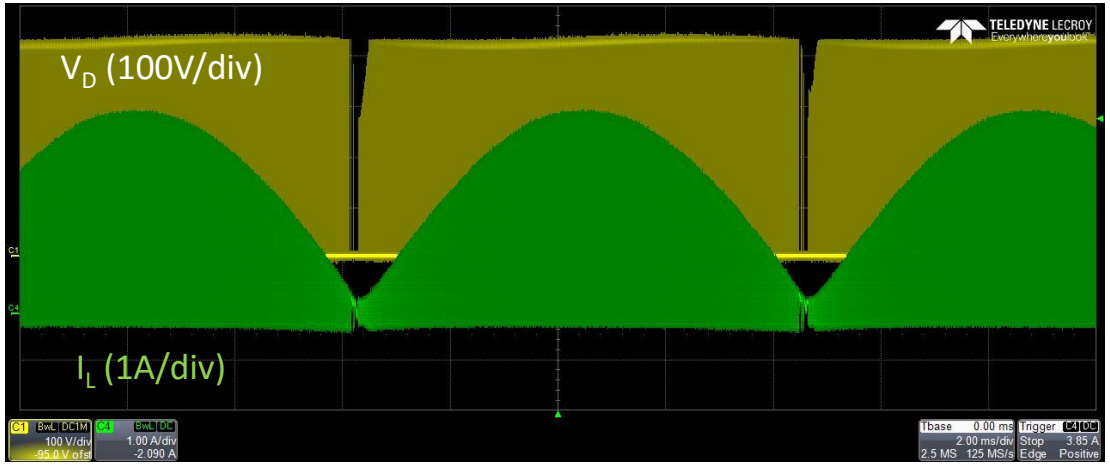




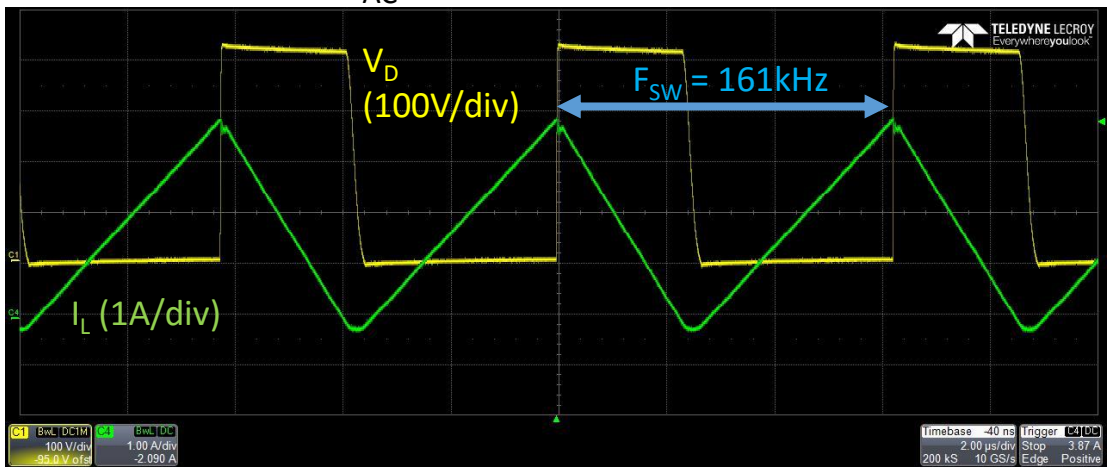
Prototype shown, under optimization

CrCM PFC: High-Frequency, High Performance

120V_{AC}, 150W

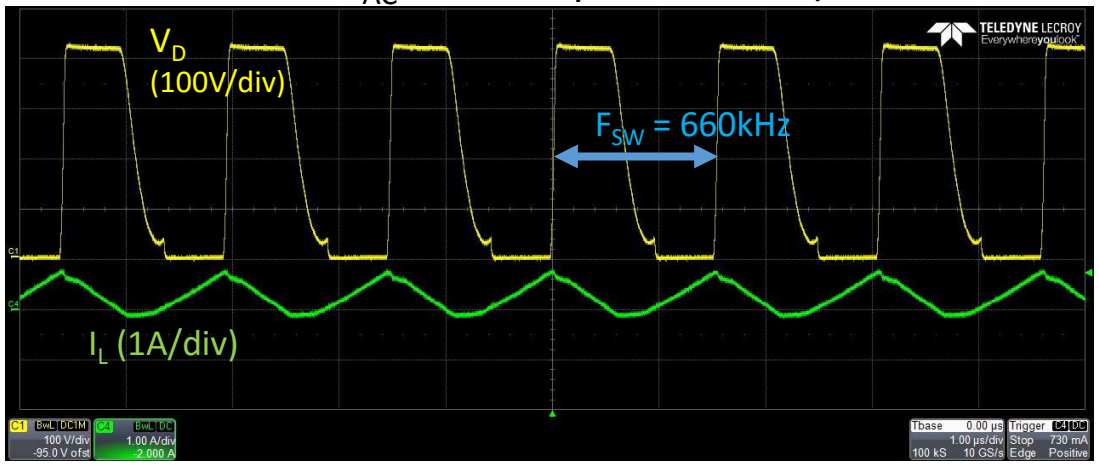


120V_{AC}, 150W, @peak AC line)

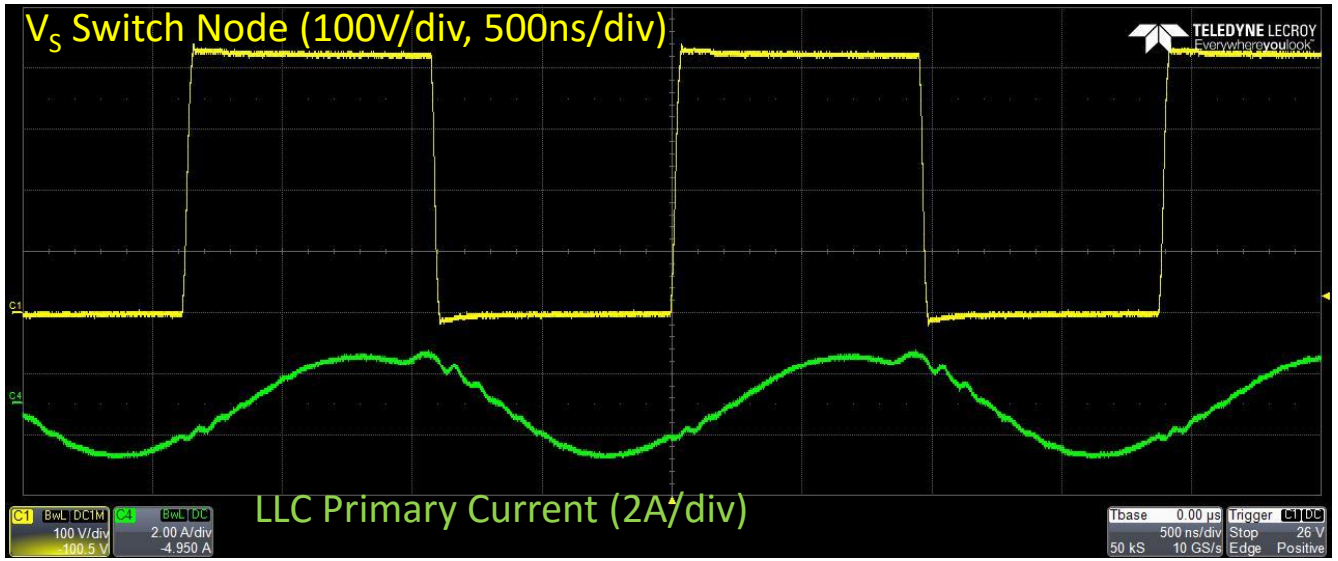


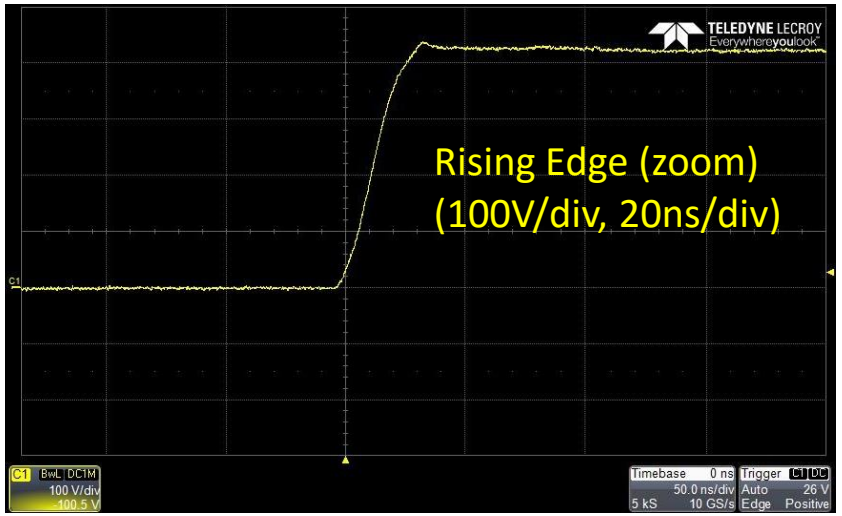
- PF >99.5%
- Efficiency 97.1% (120V_{AC}), 98.1% (220V_{AC})

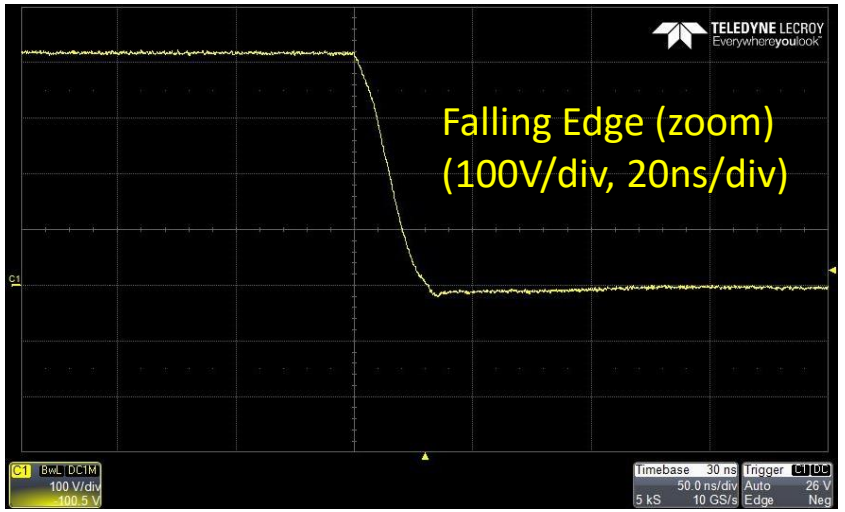
220V_{AC}, 85W, @peak AC line)



LLC: Smooth, Fast, Quiet



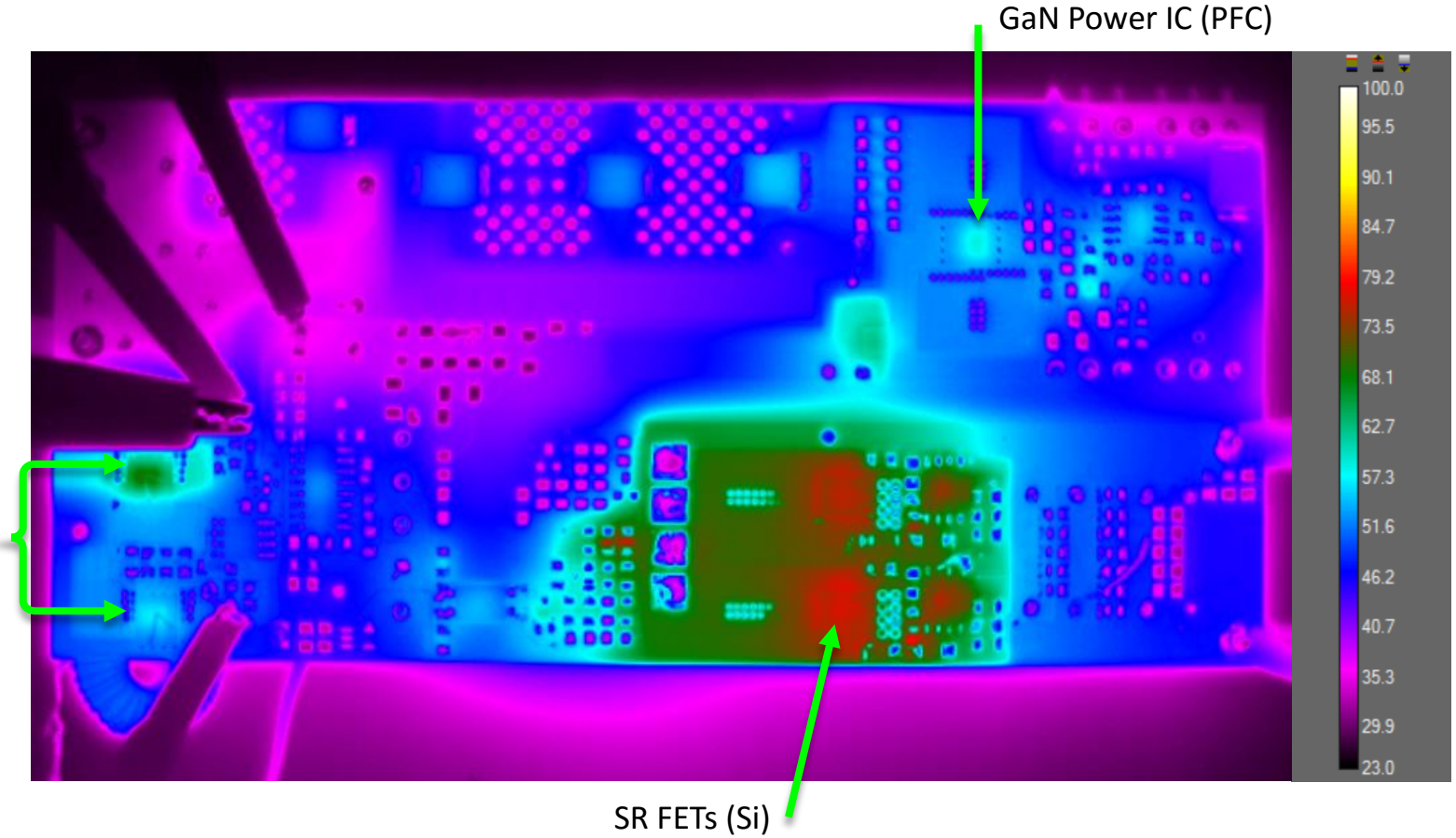




- No spikes, overshoot
- Smooth ‘S-curves’ with fast ~40V/ns slope
- Low EMI signature

GaN Power ICs: Cool at Full Load

- 120V AC_{IN}, P_{OUT} = 150W
- PFC at ~500 kHz
- LLC at ~600 kHz
- GaN Power ICs ~65°C
- Si SR FETs ~75°C



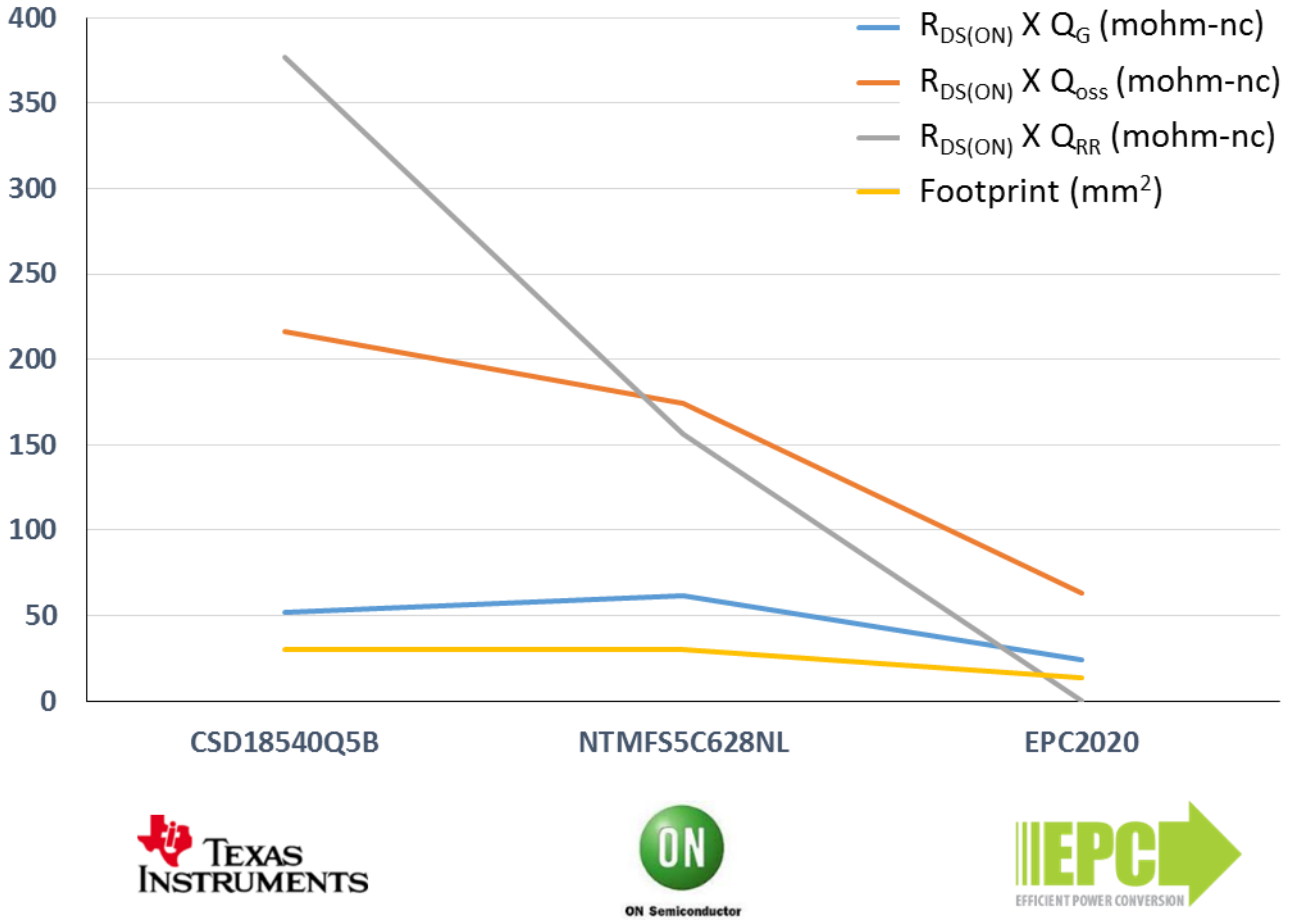
- Efficiency:

	PFC	LLC	Overall
120VAC	97.1%	94.4%	91.7%
220VAC	98.1%	94.8%	93.0%

Prototype shown, under optimization

Comparing 60V SR FETs: Better with GaN

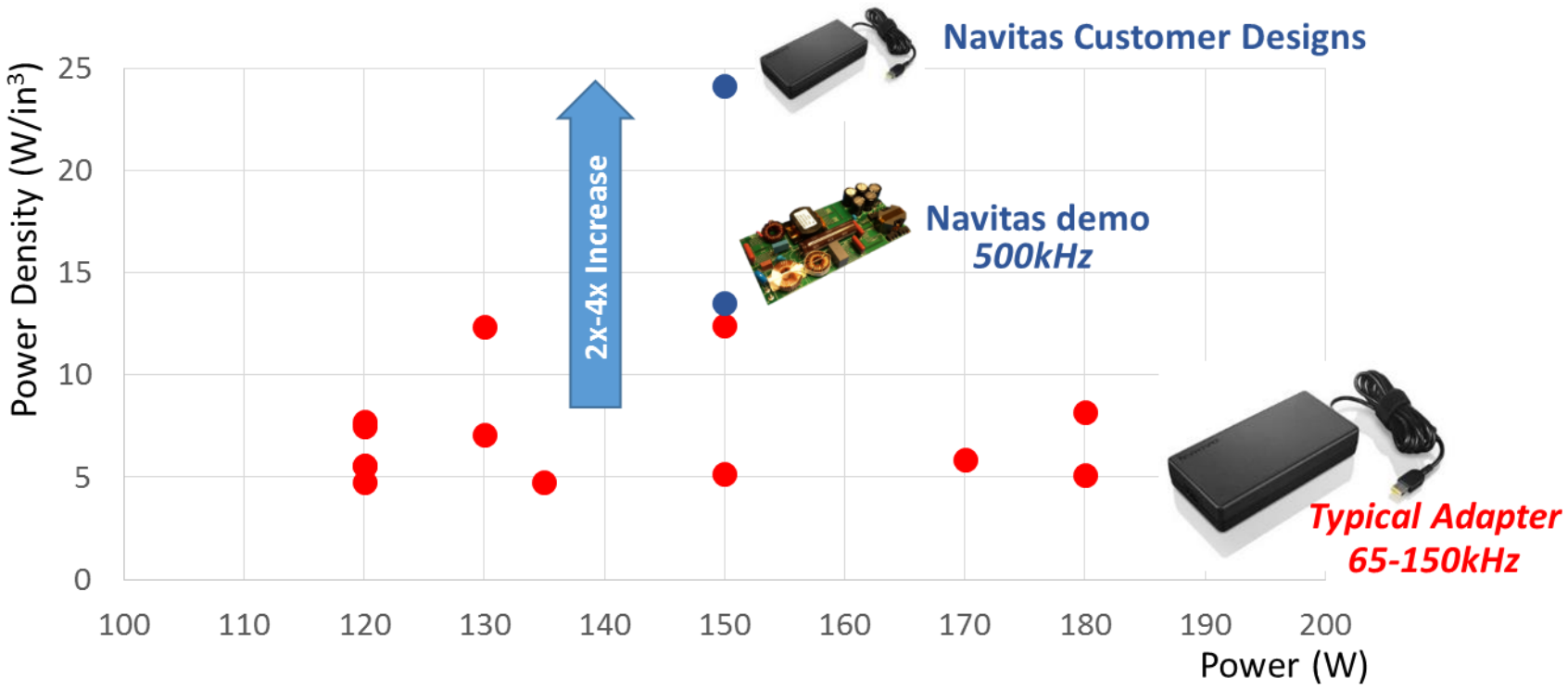
- All relevant FOMs favor GaN at 60V
  - $R_{DS(ON)}$ x Q_G reflects drive losses
  - $R_{DS(ON)}$ x Q_{OSS} reflects turn-off losses with non-resonant rectification
  - $R_{DS(ON)}$ x Q_{RR} reflects stored minority carrier turn-off losses
    (minimized with dead-time control)
- Si in QFN 5x6mm, GaN is Chip-Scale BGA



Note: Datasheet typicals at 4.5/5V gate drive and capacitance curves

Frequency drives 2x-4x Power Density

- Typical adapters (65-150kHz) = 5-12W/in^3
- Navitas demo (500kHz) = 13.5W/in^3
- Navitas customer estimate = 20-25W/in^3

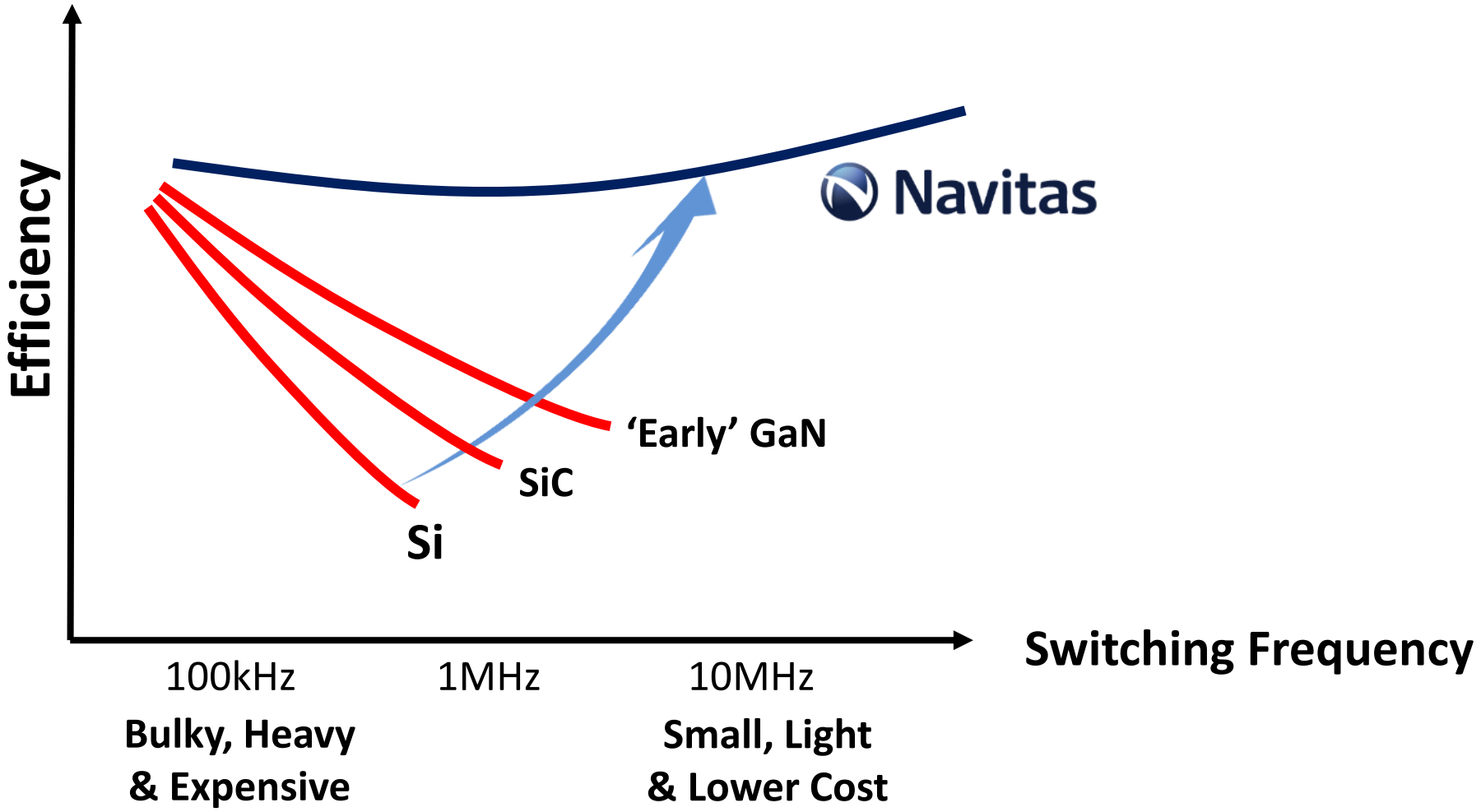


Gamer Laptops (100-150W)

All-in-One PCs (150-200W)

38”-52” TVs (100-200W)

GaN Power IC's Enable High Frequency & Efficiency



The New World…

The New World…