



GaN Reliability Through Integration and Application Relevant Stress Testing

APEC 2018 PSMA Sponsored Industry Session:
“Reliability and Ruggedness – How to Address these Challenges in Wide Bandgap Semiconductor Devices”

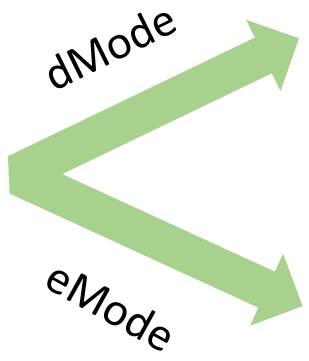
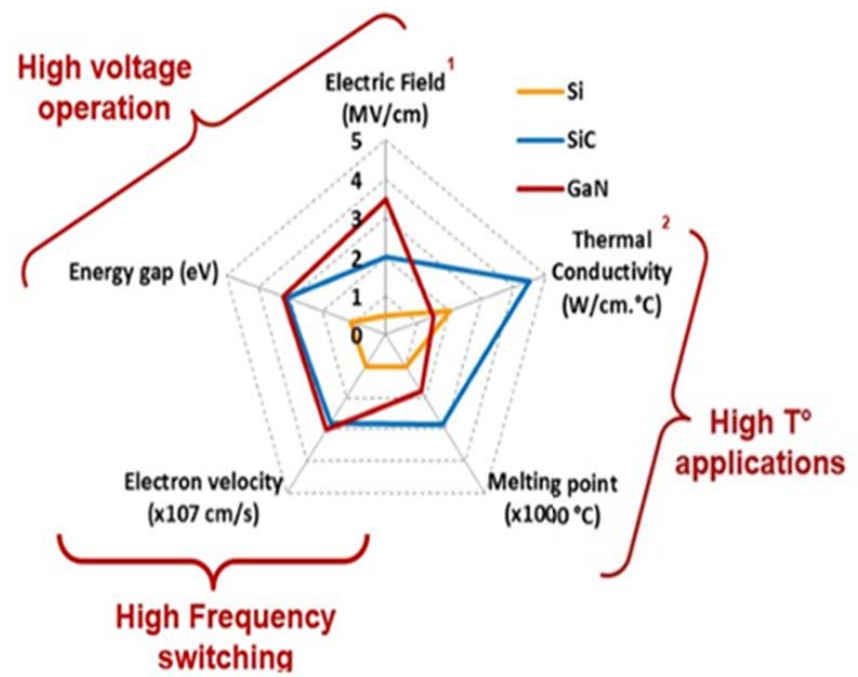
Thursday March 8th, 2018

Dr. Nick Fichtenbaum, Co-Founder & VP Engineering

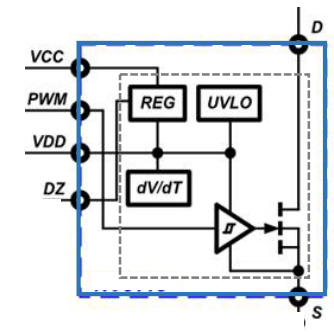
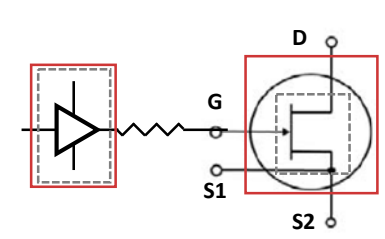
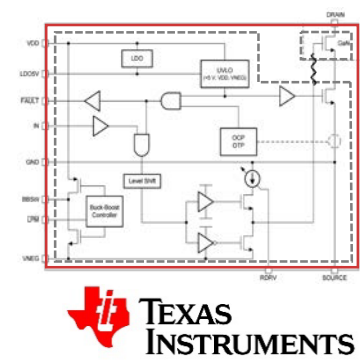
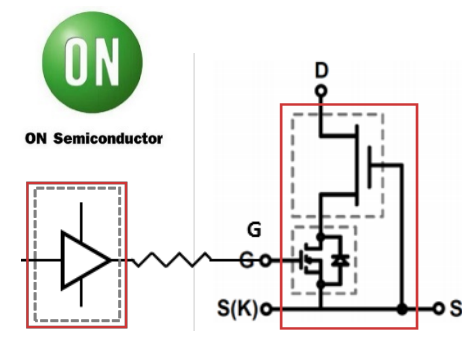
Nick.Fichtenbaum@navitassemi.com

GaN Device Implementations

Fundamental GaN Material Properties

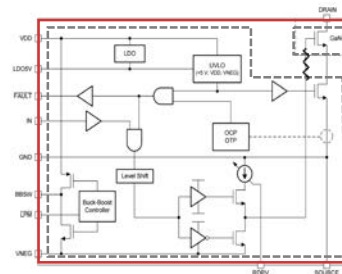
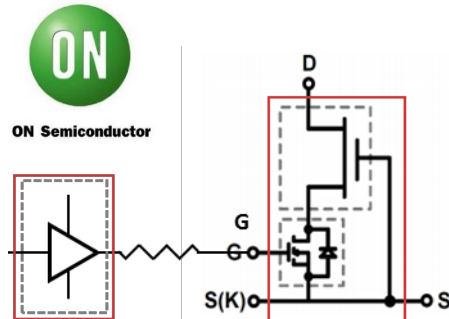


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Gate Protection is Paramount in GaN

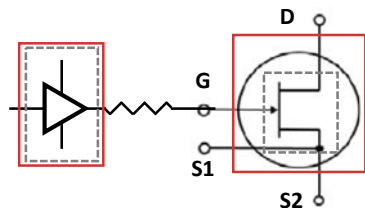
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TEXAS
INSTRUMENTS

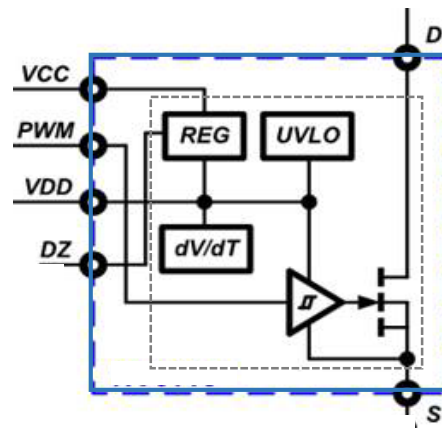
dMode (Dielectric Based Gate)

- Max V_{GS} similar to Si devices
 - Need to manage max negative gate bias on GaN for reliability
- Slew rate control important with multiple chips in a package



Panasonic infineon

GaN Systems EPC
EFFICIENT POWER CONVERSION



Navitas

eMode (pGaN Based Gate)

- V_{GS} needs to be managed
 - Clamp diodes & current based-drive
 - Layout optimization
 - GaN Power IC (integrated regulator + driver)
- C dv/dt Induced Turn-on concern
 - Negative gate drive
 - Minimize parasitics
 - GaN Power IC (integrated driver)

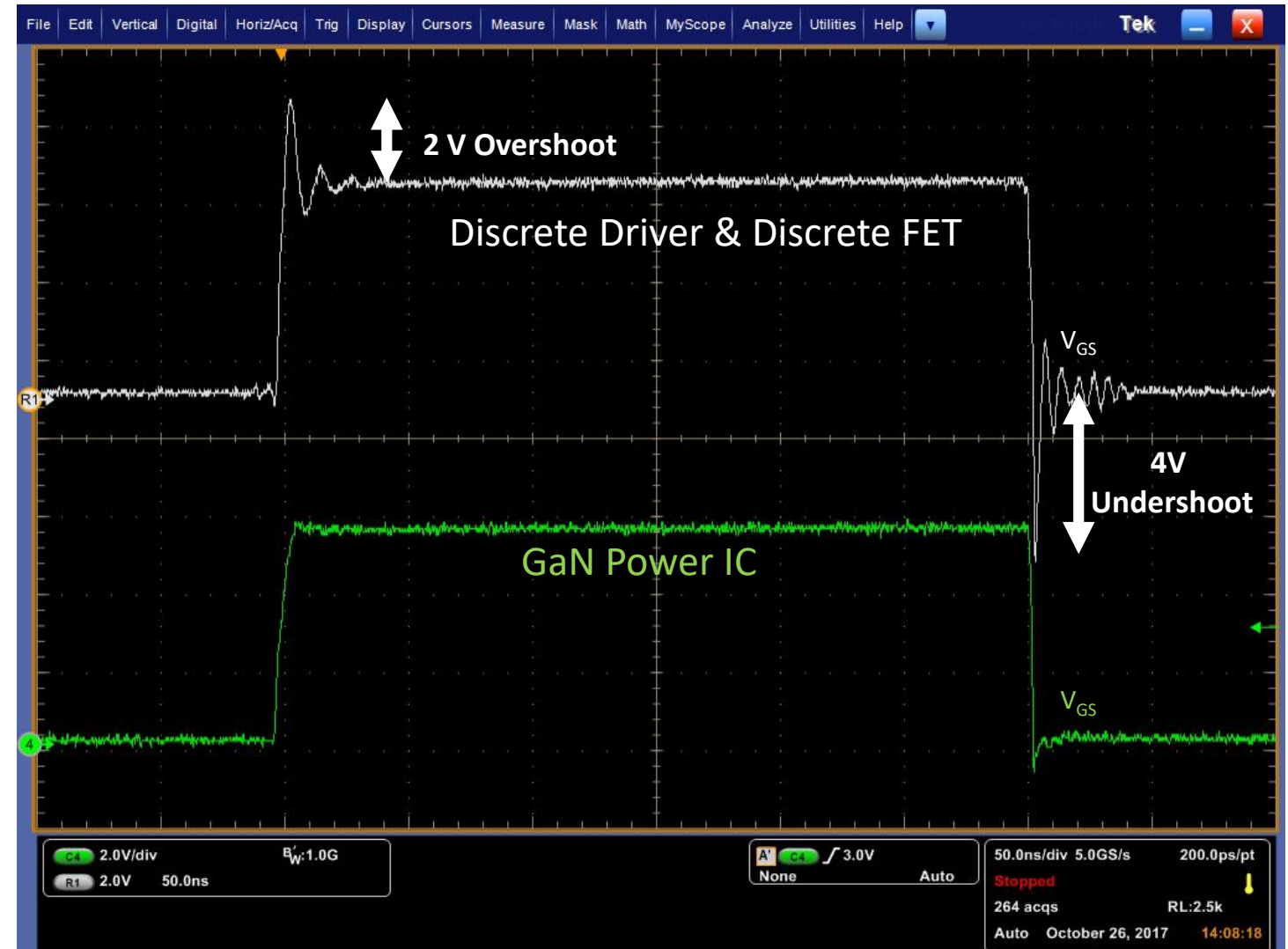
Clean, Controlled FET Gate

- **Discrete driver**

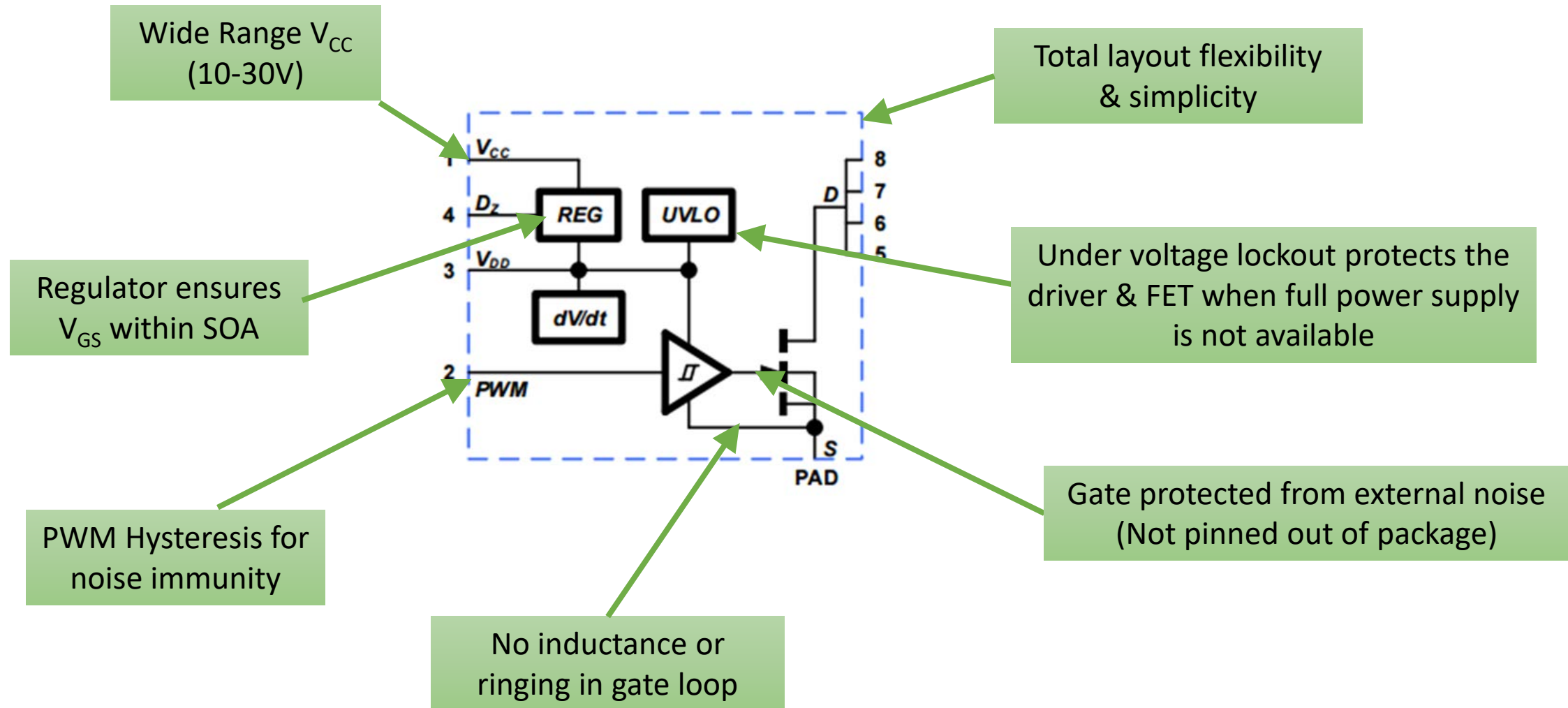
- Gate loop inductance creates overshoot (even with good layout)

- **GaNFast™ Power IC**

- No gate loop parasitic
- Clean and fast gate signal

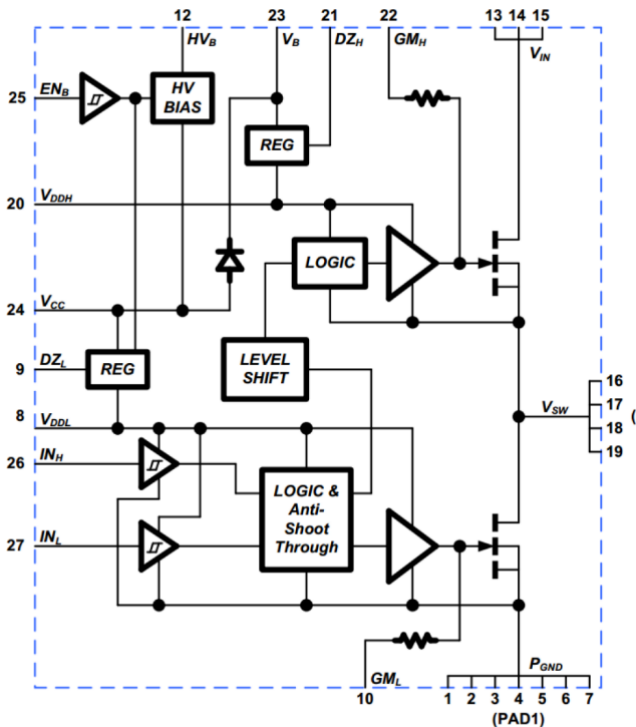


Integrated Drive → *Simple & Robust*

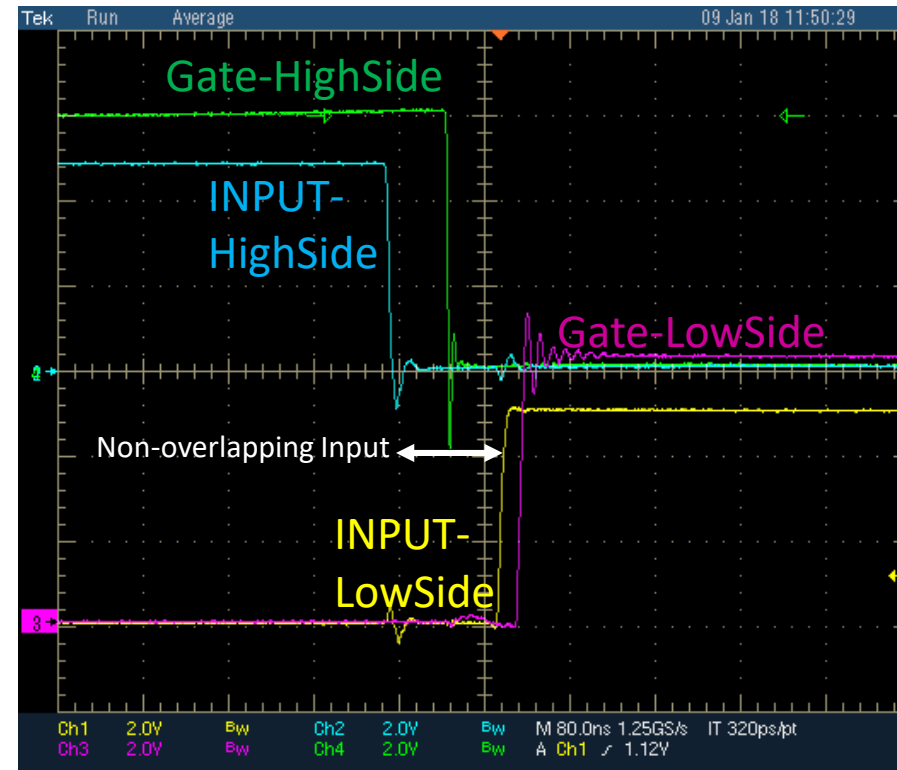


Shoot-Through Protection in Half-Bridge

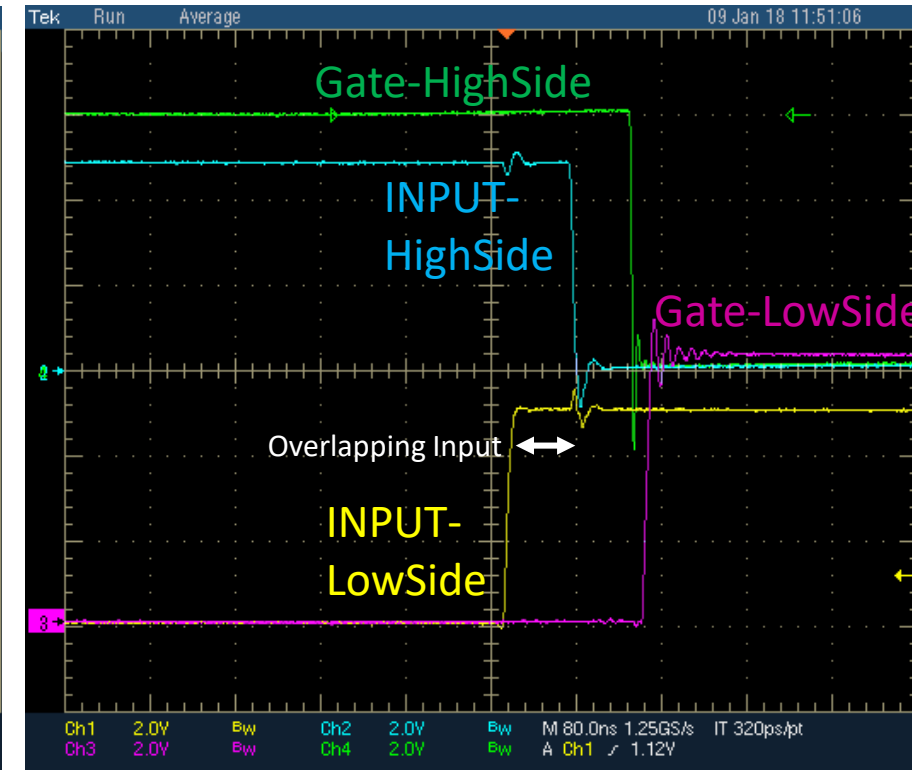
Half-Bridge GaNFast Power IC



Non-Overlapping Logic Input
(Typical Operation)



Overlapping Logic Input
(Power IC Protection Mode)



High-side and Low-side gates never overlap due to shoot-through protection in power IC

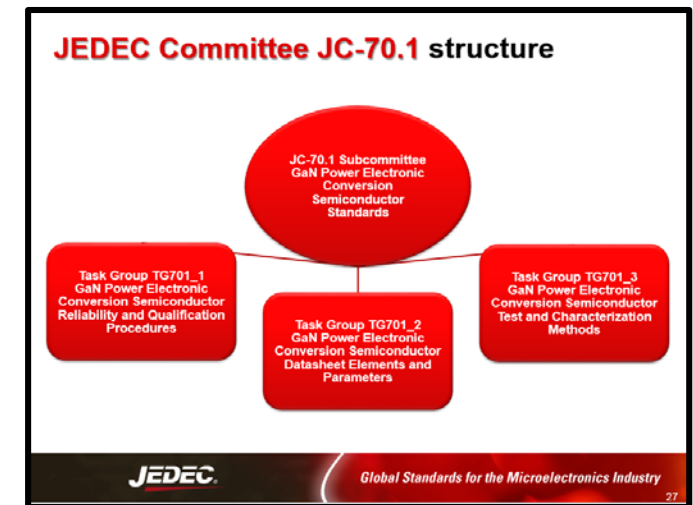
Is Typical Si JEDEC Qual Sufficient?

Typical Si-Based Qual Plan

Die Stress Package Stress	Reference	Test Conditions	Duration	Lots	S.S.
	JESD22-A113 J-STD-020	Preconditioning (MSL1): Moisture Preconditioning + 3x reflow: HAST, UHAST, TC & PC	N/A	3	308
	JESD22-A104	Temperature Cycle: -55°C / 150°C	1,000cy	3	77
	JESD22-A122	Power Cycle: Delta Tj = 100°C	10,000cy	3	77
	JESD22-A110	Highly Accelerated Stress Test: 130°C / 85%RH / 100V V _{DS}	96hrs	3	77
	JESD22-A108	High Temperature Reverse Bias: 150°C / 520V V _{DS}	1,000hrs	3	77
	JESD22-A108	High Temperature Gate Bias: 150°C / 6V V _{GS}	1,000hrs	3	77
	JS-001-2014	Human Body Model ESD	N/A	1	3
	JS-002-2014	Charged Device Model ESD	N/A	1	3

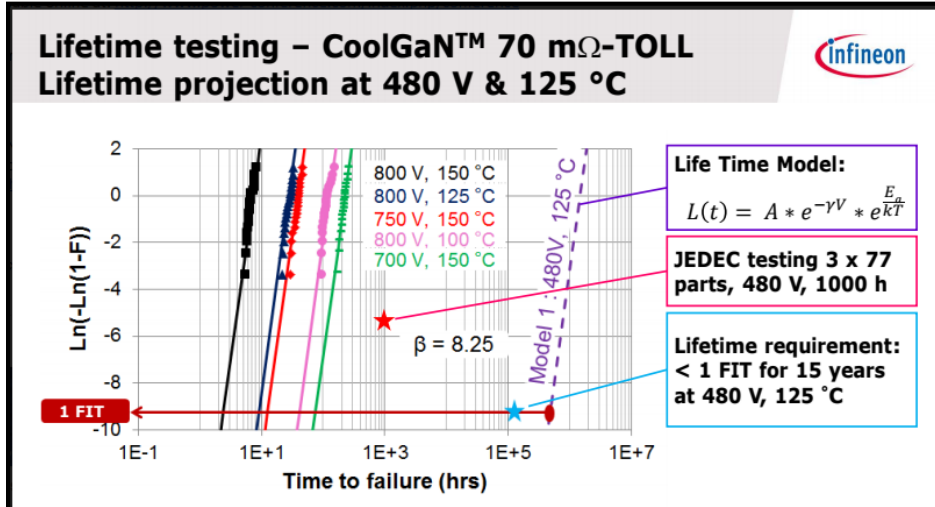


**New GaN
Standards
Needed**

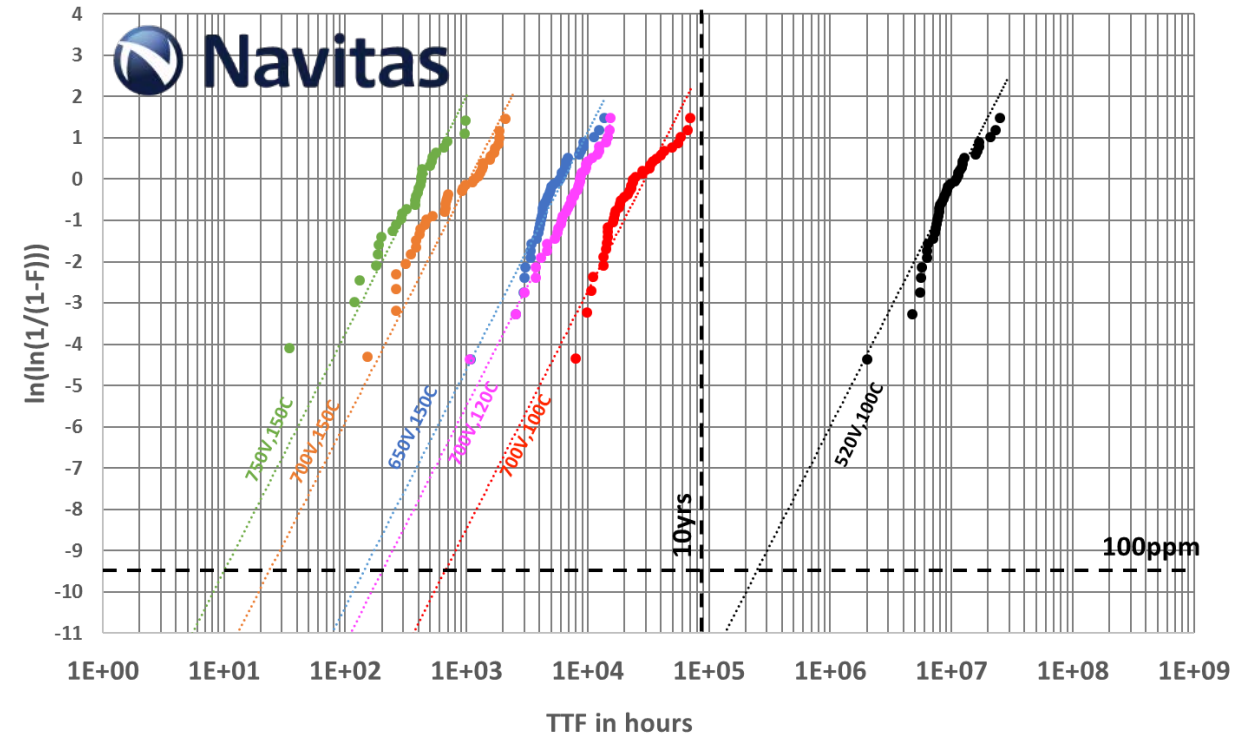
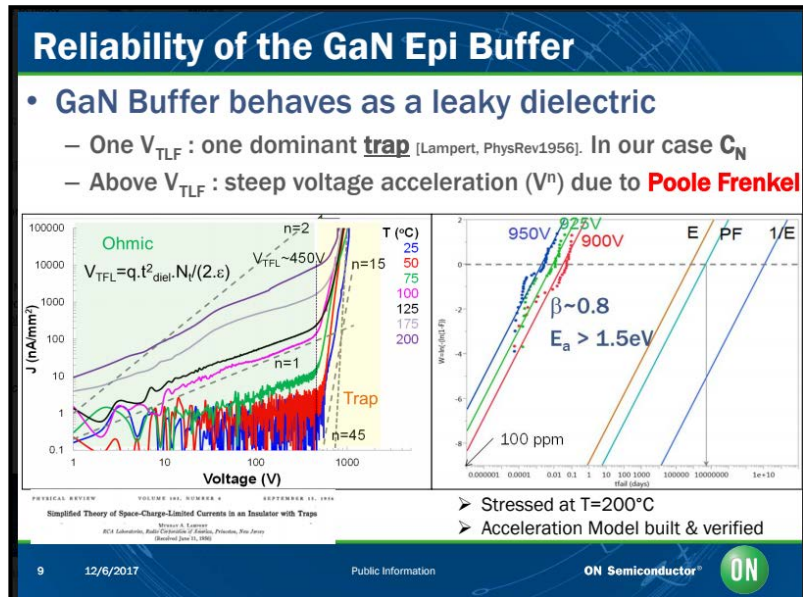


Courtesy: Stephanie Watts Butler (Texas Instruments) and Tim McDonald (Infineon) "From GaNSPEC DWG to JEDEC JC-70.1: An update on industry qualification standards for Gallium Nitride power conversion devices"

'Beyond JEDEC' -- Lifetime based on HTRB?



Bodos Power Electronics Conference 2017, Munich Airport Hilton, December 05, 2017



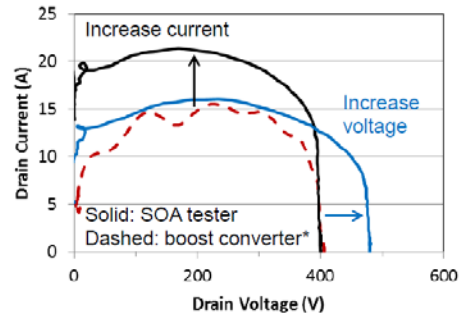
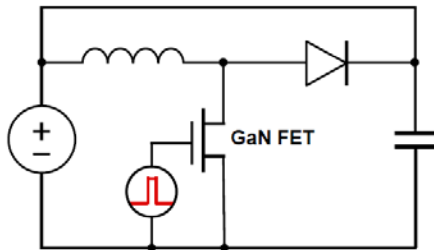
$$\text{Lifetime} = A \times (V^{-\gamma}) \times (e^{\frac{E_A}{kT}})$$

HTRB Lifetime @ 100 ppm is > 20 yrs at application condition

'Beyond' JEDEC – Implications for GaN Power ICs?

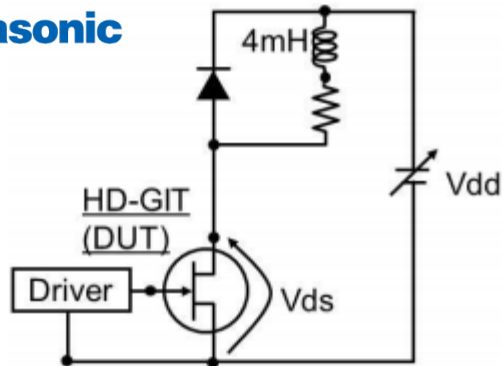
Switching SOA test-vehicle

Boost converter with output tied to input
(familiar double-pulse tester)



<http://www.ti.com/lit/wp/slyy070/slyy070.pdf>

Panasonic



How2PowerToday: September 2015 issue

transphorm

Reliability Lifecycle of GaN Power Devices

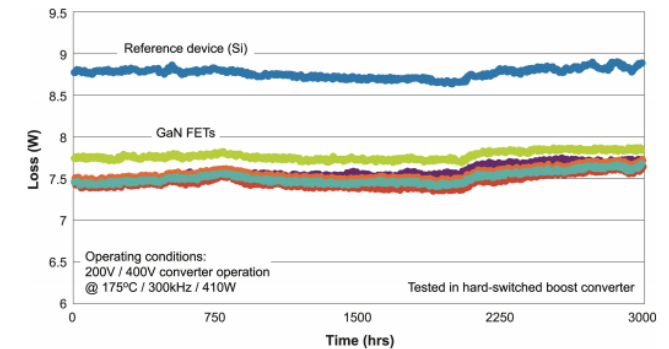
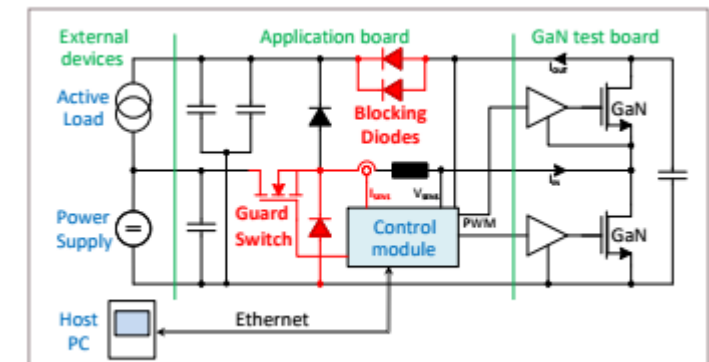


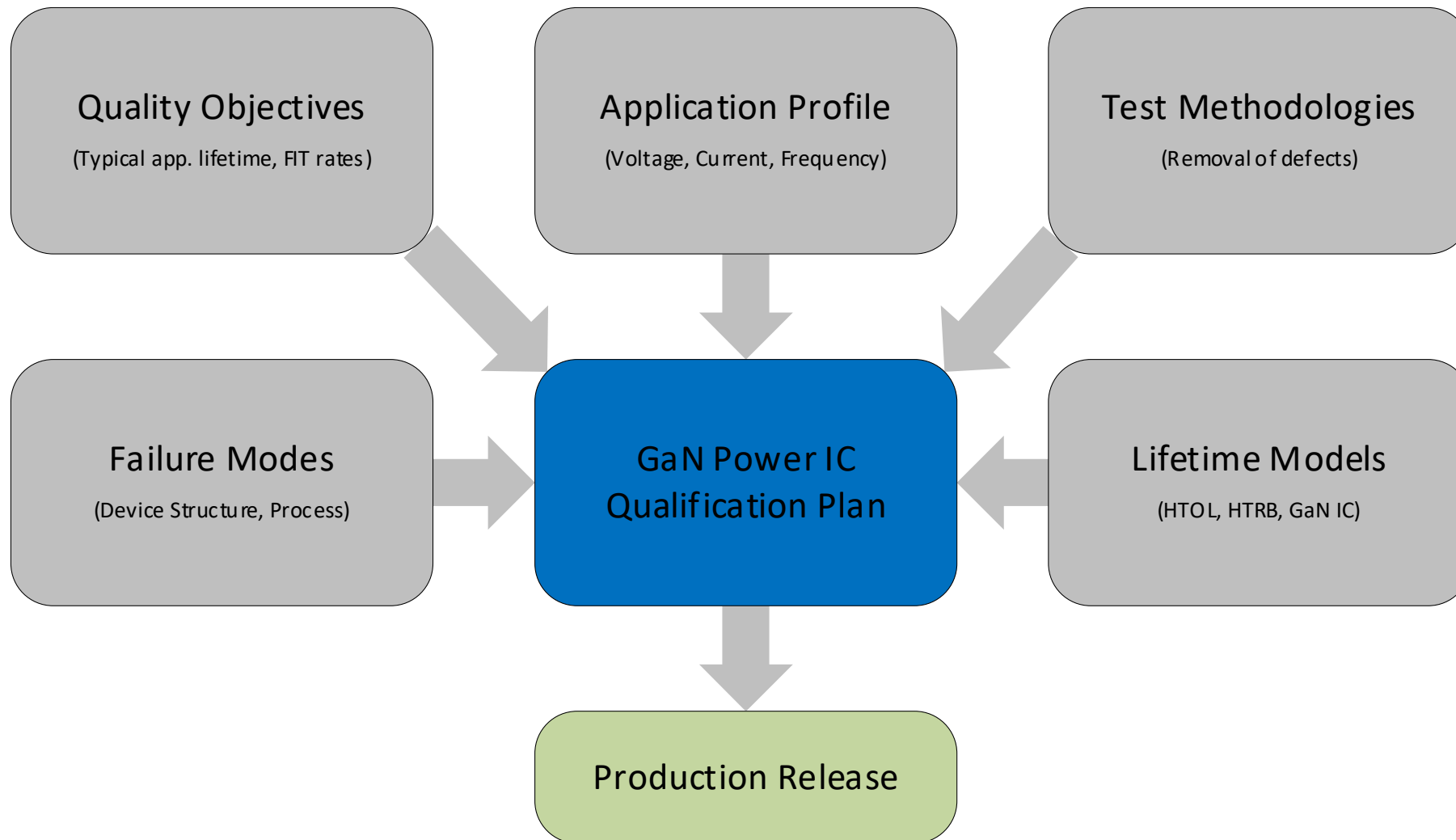
Figure 3. Loss plot for HTOL of seven 600-V-rated GaN-on-Si FETs and a reference device to 3000 hours at $T_J=175^\circ\text{C}$; each device operated in a boost converter at 300kHz with a boost ratio 200V:400V, 410W output power

<http://www.transphormusa.com/document/white-paper-reliability-lifecycle-gan-power-devices/>



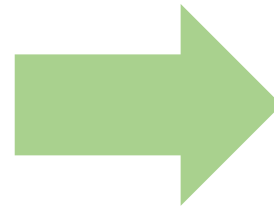
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Mission Profile Defines GaNFast Power IC Qualification

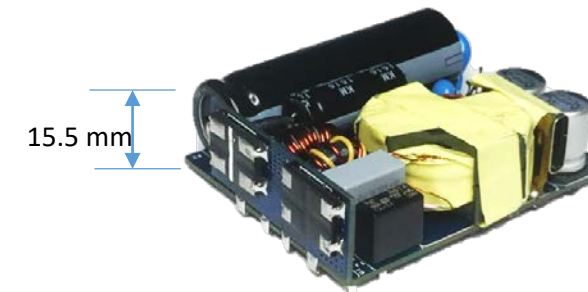
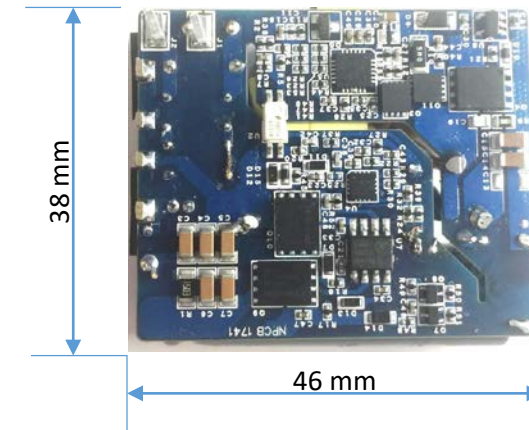


Typical Application (Consumer Chargers)

MacBook <100 kHz
 $<6.5 \text{ W/in}^3$, 92%



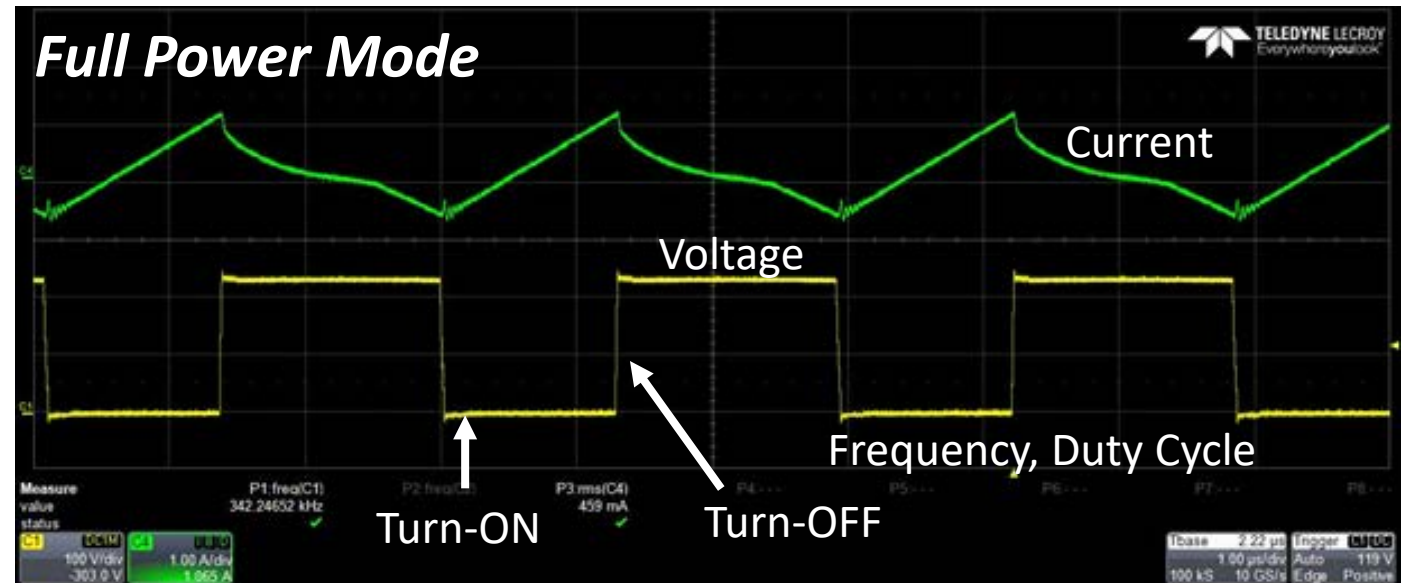
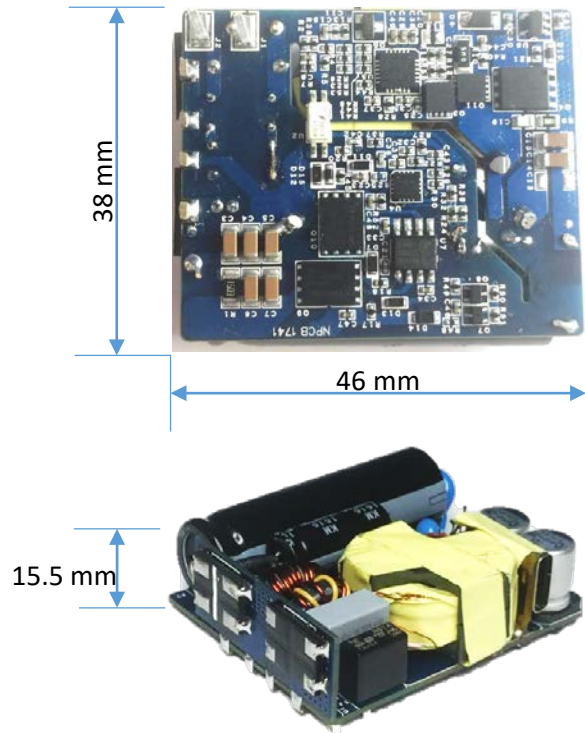
Navitas ~300 kHz
 24 W/in^3 , 94%
 = 45 cc cased



- ACF (ZVS) Topology
- 300 kHz – 1 MHz
- 120 V – 240 V_{AC}

Application Profile for ACF Charger

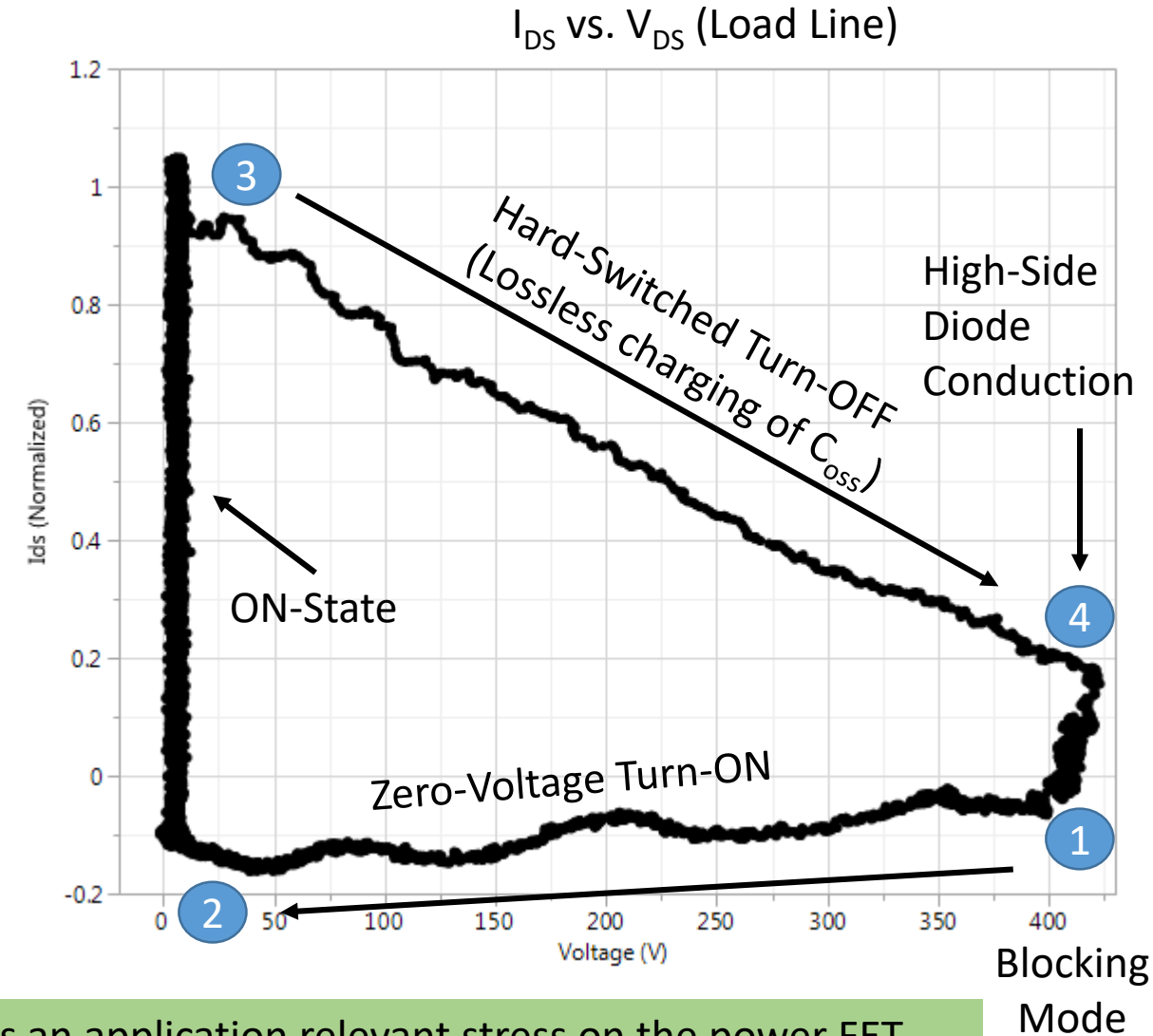
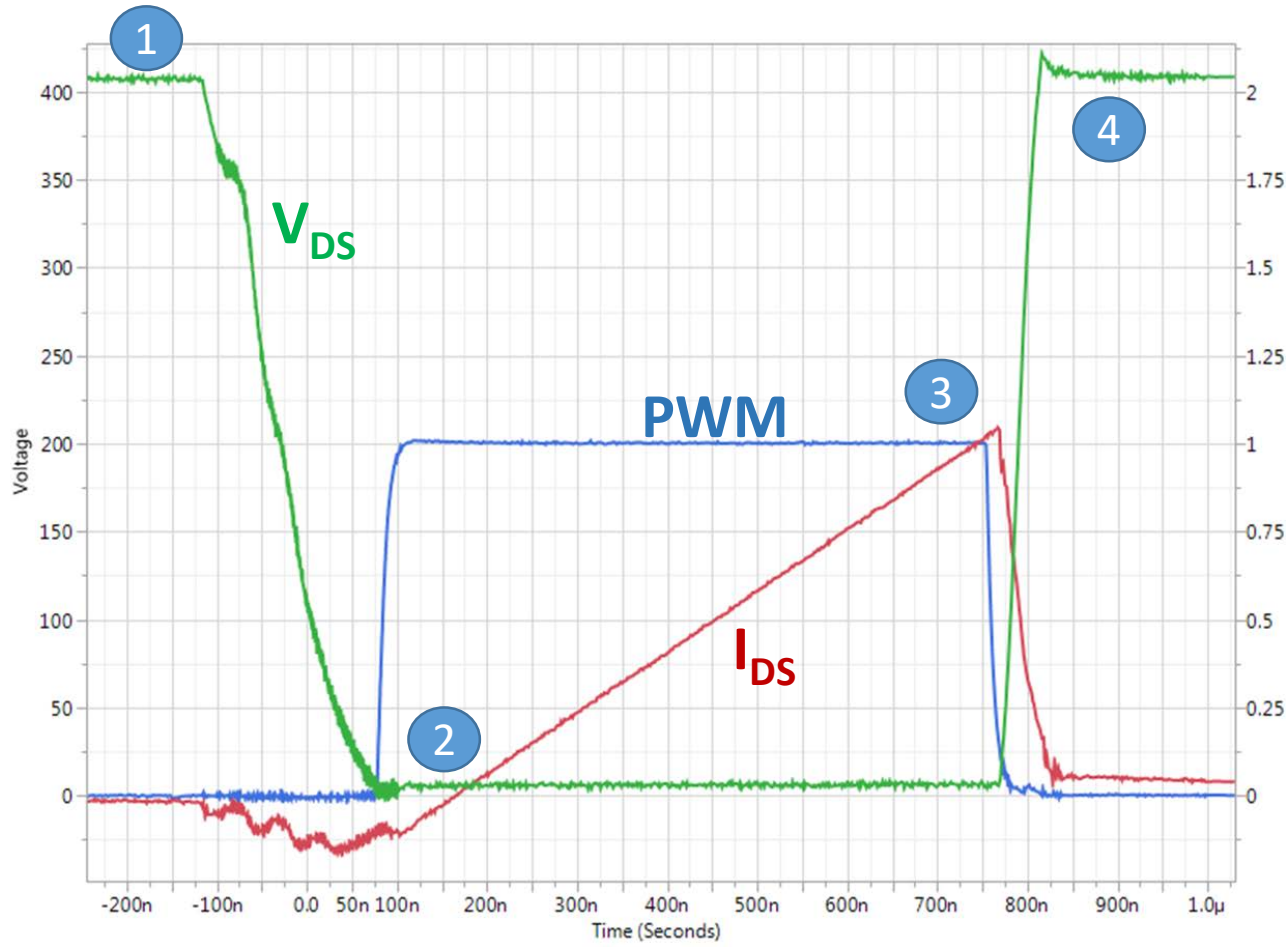
Navitas ~300 kHz
 24 W/in³, 94%
 = 45 cc cased



Application Factors

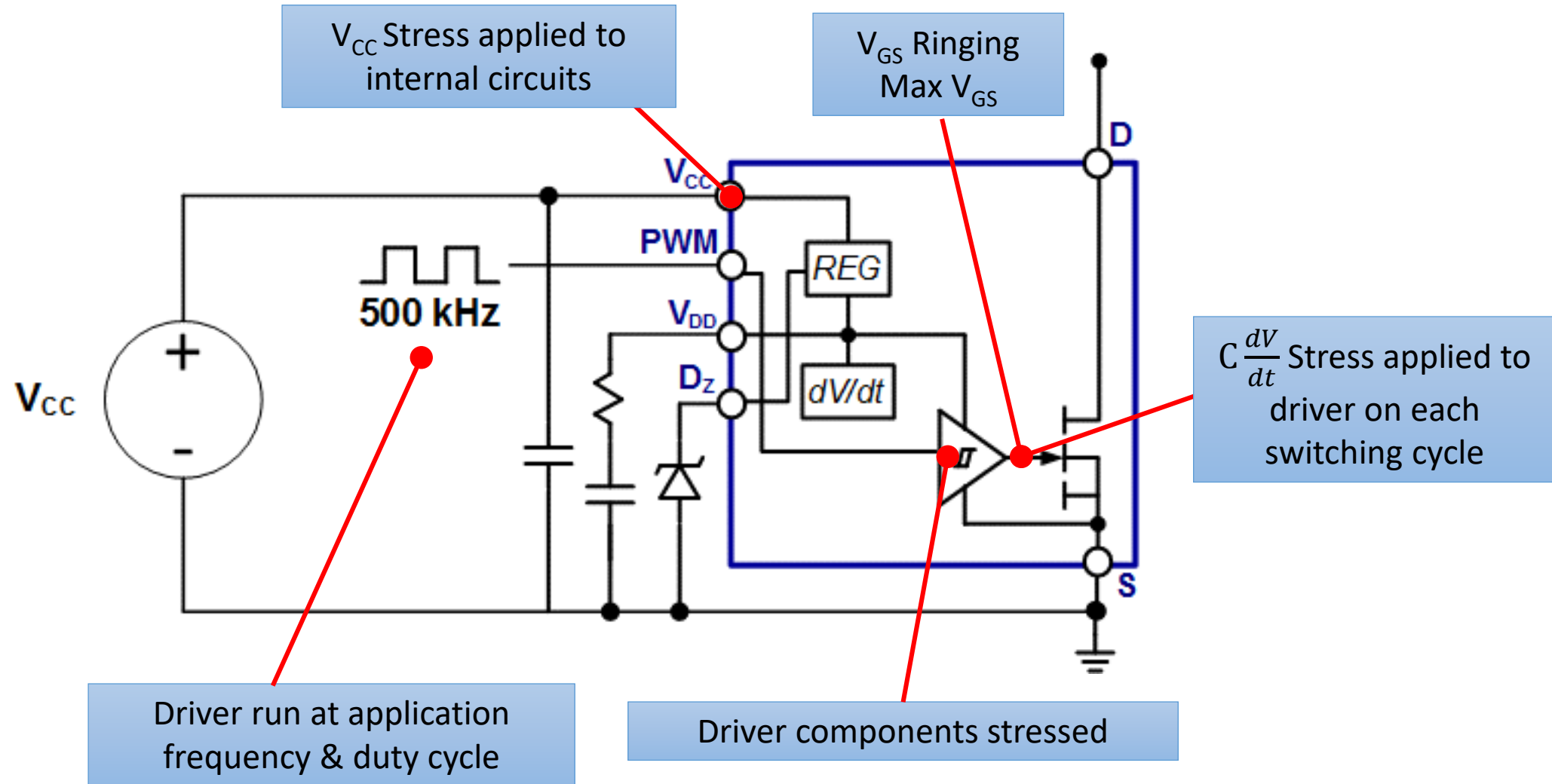
- Voltage (300 – 480 V)
- Current (1-3 A)
- Frequency (100-1,000 kHz)
- Temperature (25 – 100 C)
- Duty Cycle
- Turn-on / Turn-off Profile
- ZVS vs. Hard-Switching

ZVS Application Profile (FET)

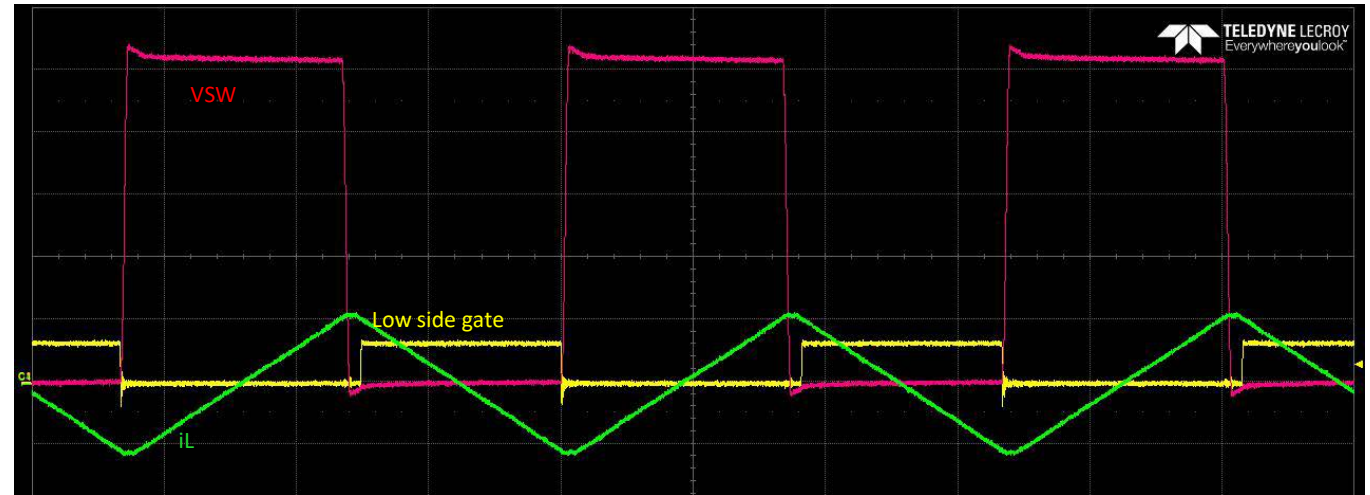
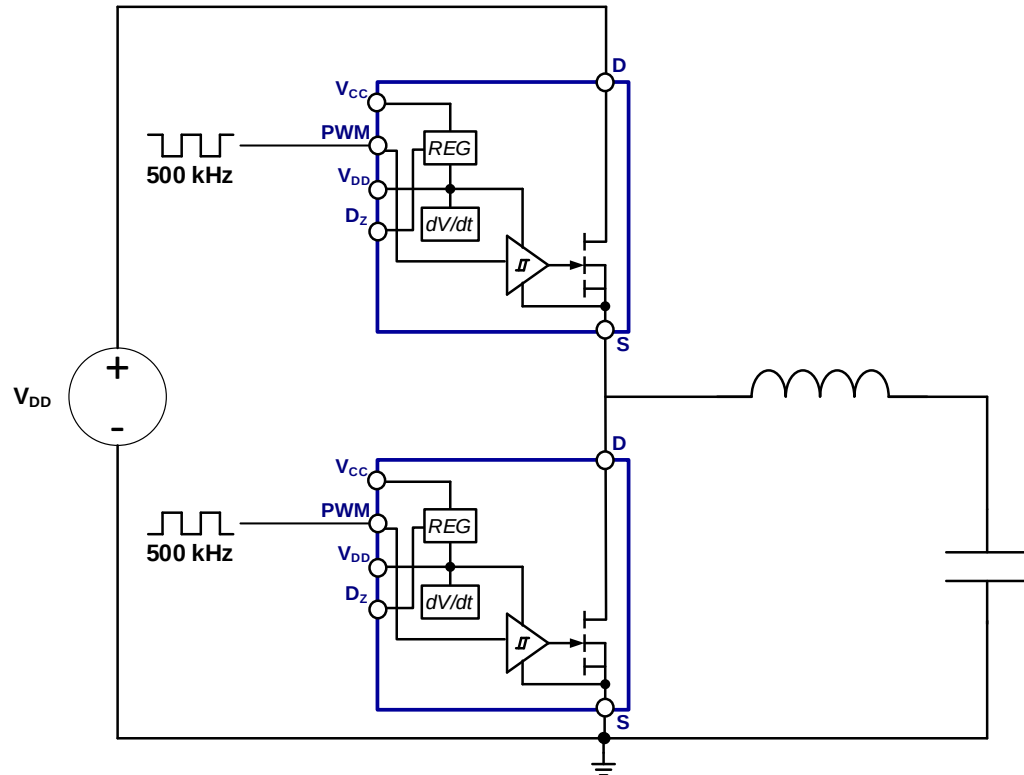


'Soft-Switching' or ZVS (Zero-Voltage Switching) represents an application relevant stress on the power FET

ZVS Application Profile (IC)



ZVS High Temp Op Life (HTOL) Circuit



HTOL Circuit Variables

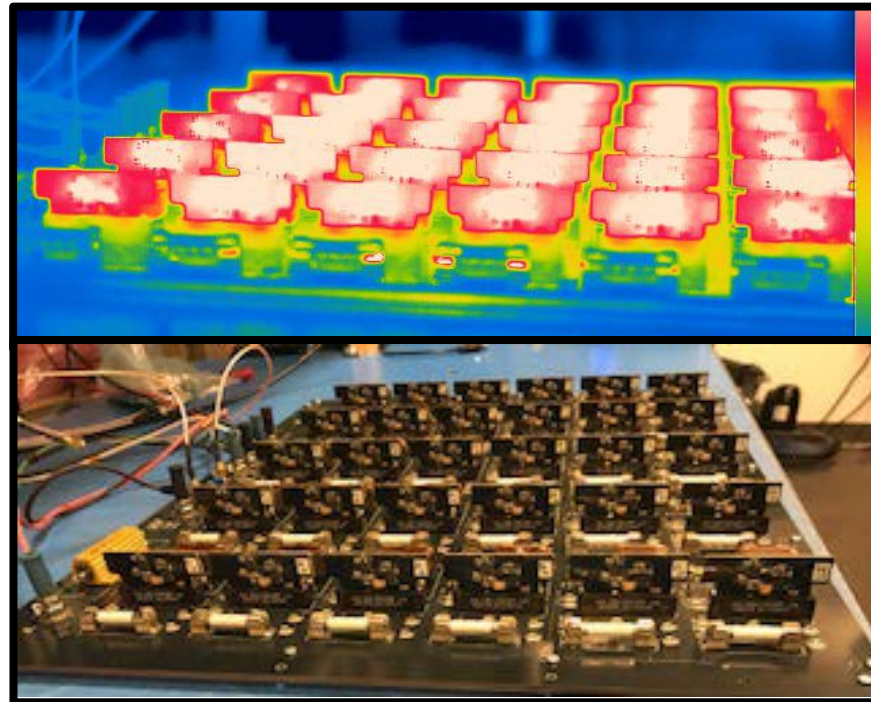
- | | |
|---|---|
| <ul style="list-style-type: none"> • Voltage • Current • Frequency | <ul style="list-style-type: none"> • Temperature • Duty Cycle |
|---|---|

- L-C load applied to half-bridge topology along with complementary inputs & dead time setting to achieve soft-switching
- Power consumption is the only loss elements (DUT, Inductor) since energy is recycled → many cells in parallel
- Circuit allows for same application stress on GaNFast Power IC as customer application (Voltage, Current, Frequency)
- Applies application conditions to the driver & integrated IC so power IC is also qualified in the same test

ZVS HTOL Applied to Statistical Sample Sizes

HTOL Mother Board

- Matches all elements of application profile
 - FET & IC
- Many cells in parallel
 - Statistical sample sizes
- Low total power consumption
- Conditions changeable to develop lifetime and acceleration models



Qualification

3 Lots x 77 Parts

Lifetime Models

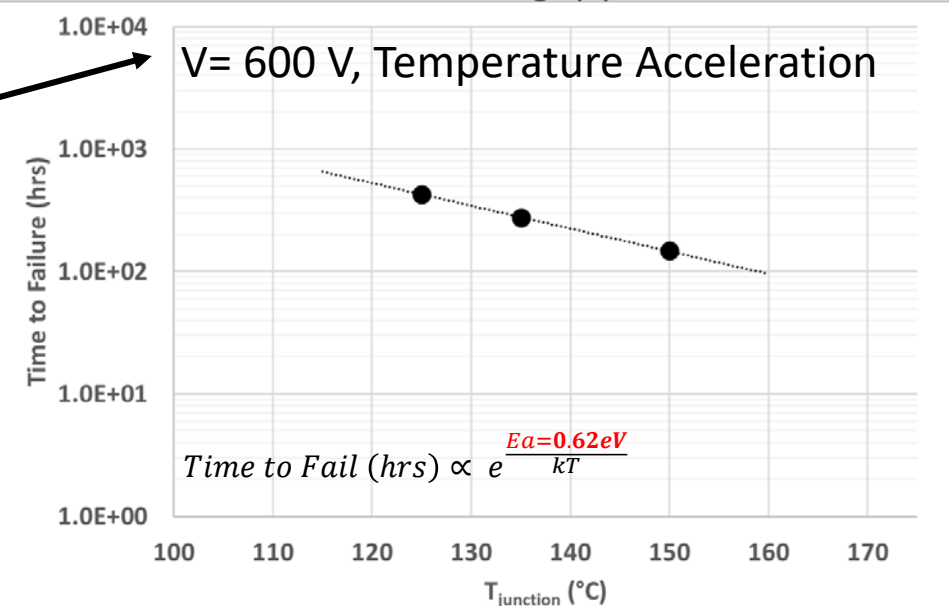
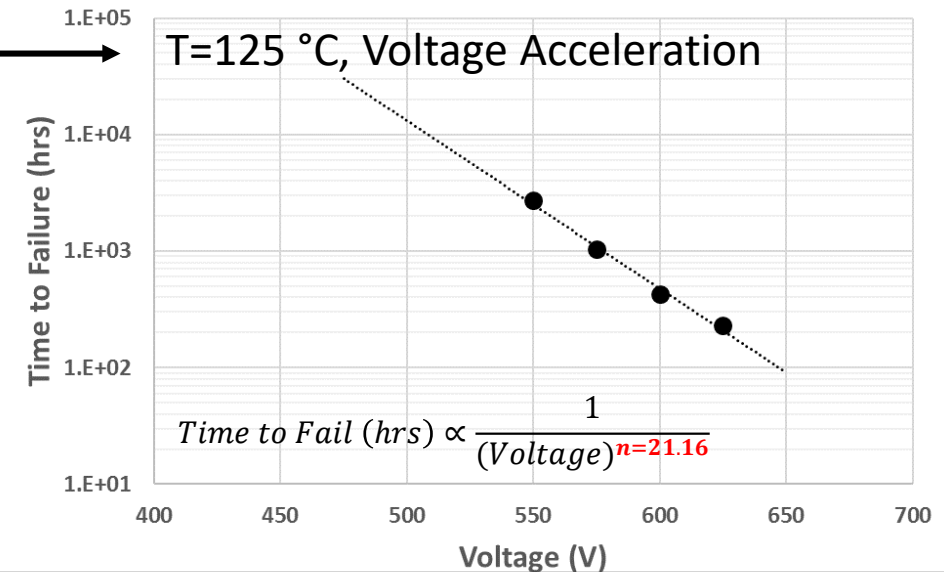
Voltage
Current
Frequency
Temperature

Early Life
Failure Rate

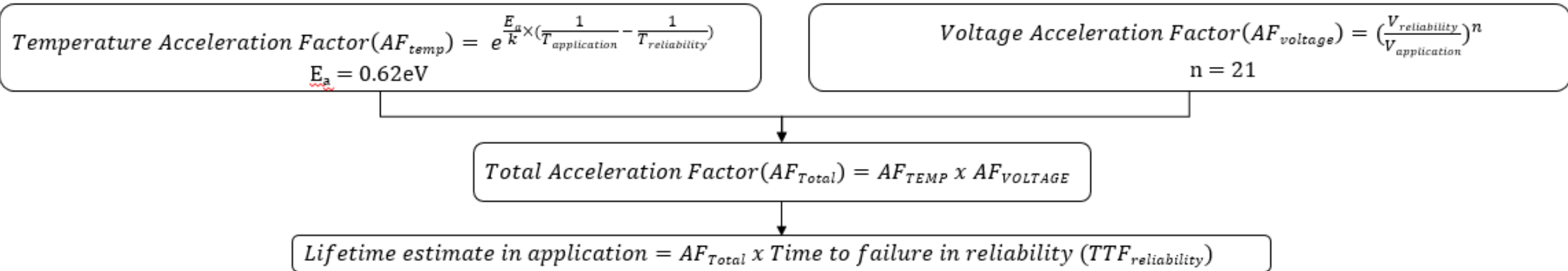
3 Lots x 1,000 Parts

HTOL-based Lifetime Model

Voltage/ Temperature	125	135	150
550	✓		
575	✓		
600	✓	✓	✓
625	✓		



Lifetime Estimation in Charger Application (ACF)



ACF Charger
Full-Power
Profile →

AC line Voltage (V)	Rectified AC voltage (V)	Reflected Voltage (V)	Switch Voltage (V)	Full power Temp (°C)
120	170	125	295	85
240	340	125	465	85

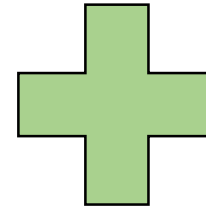
$$\text{Lifetime} = AF_{Total} \times TTF_{reliability} = \mathbf{81 \text{ years}} @ 240V \text{ AC input}$$

Predicted lifetime in charger application (ACF) exceeds 10yr lifetime requirement

'Beyond' JEDEC Qual Plan for GaN

GaN-Based Qual Plan

	Reference	Test Conditions	Duration	Lots	S.S.
Package Stress	JESD22-A113 J-STD-020	Preconditioning (MSL1): Moisture Preconditioning + 3x reflow: HAST, UHAST, TC & PC	N/A	3	308
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Die Stress	JESD22-A108	High Temperature Reverse Bias: 150°C / 520V V _{DS}	1,000hrs	3	77
	JESD22-A108	High Temperature Gate Bias: 150°C / 6V V _{GS}	1,000hrs	3	77
	JESD22-A108	High Temperature Operating Life	1,000hrs	3	77
	JS-001-2014	Human Body Model ESD	N/A	1	3
	JS-002-2014	Charged Device Model ESD	N/A	1	3



Lifetime Models
(HTOL, HTRB)

Failure Modes
Established

Application Specific HTOL Test Bench