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Overview of IEEE802.3bt Power over Ethernet with Dual-signature PDs

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Introduction to IEEE Std 802.3bt™-2018 dual-signature PDs

IEEE Std 802.3bt-2018 introduces Clause 145 to the 802.3 standard and specifies two different but equally interoperable PD configurations: single-signature and dual-signature. IEEE802.3af and IEEE802.3at, the PoE standards that preceded IEEE Std 802.3bt™-2018, did not define or distinguish between single-signature and dual-signature PDs, so these are important new concepts for designers and manufacturers of PoE equipment. As such, this white paper seeks to serve as a primer for the operation of dual-signature PDs, while the following white paper covers single-signature PDs and the IEEE Std 802.3bt™-2018 standard in general: https://ethernetalliance.org/wp-content/uploads/2018/04/WP_EA_Overview8023bt_V2_FINAL.pdf

At a high level, a dual-signature PD has two separate detection circuits and two separate classification circuits. In contrast, a single-signature PD has a single detection circuit and a single classification circuit. Another characteristic that distinguishes dual-signature PDs from single-signature PDs is supported load configurations. While both PD variants can be single-load (i.e. each two pairs of the same polarity are connected at some point after the diode bridge, as shown in Figure 1, only a dual-signature PD can be dual-load by keeping isolation between each two pairs of the same polarity as shown in Figure 2.

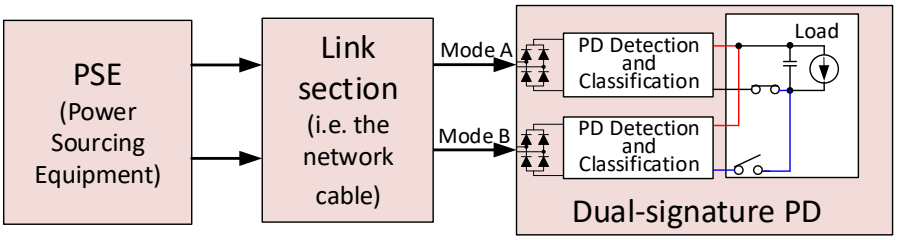

Figure 1: High-level block diagram of a PoE system with a single-load dual-signature PD

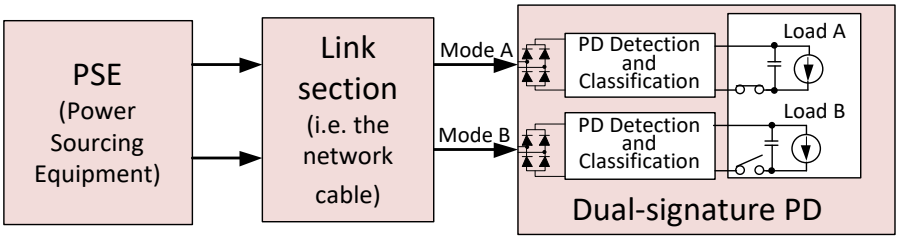

Figure 2: High-level block diagram of a PoE system with a dual-load dual-signature PD

Dual-signature PDs enable applications that require up to the same maximum power level as single-signature PDs, but with the additional flexibility of different load configurations and either a parallel or staggered power-up sequence across Modes. The following are typical applications for dual-signature PDs:

- A PD that consists of two independent, isolated loads with distinct Class requested over each Mode.
- A PD that consists of two independent, isolated loads with the same Class requested on both Modes and where only one of the loads is operating while the other provides redundancy.

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About this document

This document provides an overview of how the IEEE Std 802.3bt™-2018 Power over Ethernet standard specifies operation with dual-signature PDs. The focus of this whitepaper is on dual-signature PDs and PSE operation when powering a dual-signature PD. Important differences between dual-signature PDs and single-signature PDs are highlighted where deemed helpful. This document assumes a baseline level of understanding of the standard that can be attained by first reading the following excellent EA white paper: https://ethernetalliance.org/wp-content/uploads/2018/04/WP_EA_Overview8023bt_V2_FINAL.pdf

The information herein is based on the published version of the standard: IEEE Std 802.3bt™-2018. While every effort is made to provide correct information, there is always the inherent risk of unintentionally deviating from what the specification actually says. Thus, this white paper is intended to help understand dual-signature operation and requirements, but should not be used in lieu of the standard.

IEEE Std 802.3bt™-2018 is available from https://standards.ieee.org/project/802_3bt.html

Each major section in the document highlights the relevant portions in the IEEE Std 802.3bt™-2018 standard by listing these in a green box at the beginning of the section.

When information is presented in tabular form, an "X" means "not supported", while "√" indicates support. Also, unless specifically mentioned otherwise, references to “PSE” and “PD” without a specified Type refer to Type 3 and Type 4 devices.

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1. A dual-signature system overview

This white paper details the Power over Ethernet system that consists of a PSE connected to a dual-signature PD through a link section, as depicted in Figure 3. As with any PoE system, the PSE delivers power to the PD through the network cable, and the PD consumes the power sourced by the PSE over Mode A, Mode B, or both.

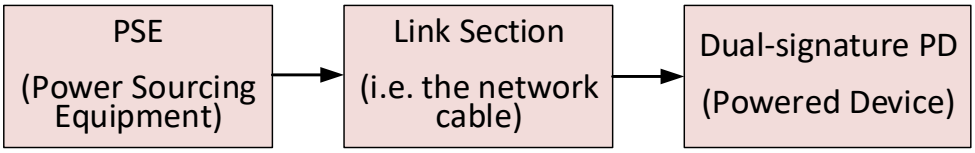

Figure 3: Power over Ethernet system with dual-signature PD

The behavior and performance of the system is largely a function of the Type of the PSE and PD, as well as the assigned and requested Class of the PSE and the PD, respectively. Type and Class are covered in detail in the following two subsections.

1.1. Type

An overview of Type in the context of dual-signature operation is helpful, as Type indicates several key characteristics of both a PSE and a PD. For example, the requirement for minimum supported Class by a PSE is a function of Type, as shown in Table 1. (Note that PSEs are not required to support the maximum Class of the given Type.)

Table 1: Supported Classes for a given PSE Type

PSE Type	Pairs operating	Class support requirements per pairset
1	2 pairs	Must support at least Class 1 and may support up to Class 3
2	2 pairs	Must support at least Class 4
3	2 pairs	Must support at least Class 1 and may support up to Class 4
	4 pairs	Must support at least Class 1 and may support up to Class 4
4	2 pairs	Must support Class 4
	4 pairs	Must support at least Class 4 and may support up to Class 5

Other PSE and PD characteristics connected to Type are shown in Table 2 and Table 3, respectively.

Table 2: PSE Type overview when connected to a dual-signature PD

Type	2-/4-pair	Max power per pairset	Max Class per pairset	Physical layer classification	Autoclass	Short MPS	Unbalance requirements
3	4	30 W	4	✓	X	✓	✓ (Note 1)
	2 (Note 2)	30 W	4	✓	X	✓	X
4	4	45 W	5	✓	X	✓	✓ (Note 1)

Note 1: See pair to pair unbalance requirements when powering dual-signature PDs in Section 6.
Note 2: A 2-pair PSE, when connected to a dual-signature PD, is only capable of providing power to one of the Modes, where the Mode that will be powered is either mode A or Mode B.

Table 3: Dual-signature PD Type overview

Type	Max power per pairset	Max total power	Classes	LLDP	Autoclass	Short MPS	Unbalance requirements
3	25.5 W	51 W	1 to 4	✓ (Note 2)	X	✓	✓ (Note 1)
4	35.6 W	71.3 W	1 to 5	✓	X	✓	✓ (Note 1)

Note 1: See pair to pair unbalance requirements in section 6.
Note 2: Only when either Class ≥ 4.

1.2. Class

Class is another important concept in the Power over Ethernet standard, as it defines the maximum power that can be sourced or drawn in the system. Table 4 shows the power Classes defined per Mode by IEEE Std 802.3bt™-2018 for Type 3 and Type 4 dual-signature PDs. A power Class assigned per Mode provides the flexibility for dual-signature PDs to have different Classes between Modes. Yet, the maximum power that a Type 4 dual-signature PD may consume over four pairs is the same as that of a Type 4 single-signature PD (i.e. 71.3 W = 2 * 35.6 W).

Table 4: Power Classes per pairset defined by IEEE Std 802.3bt™-2018 for dual-signature PDs

IEEE Std 802.3bt™-2018 Type 3				IEEE Std 802.3bt™-2018 Type 4
PSE (over each Alternative)				
Class 1 = 4 W	Class 2 = 7 W	Class 3 = 15.4 W	Class 4 = 30 W	Class 5 = 45 W (1)
PD (over each Mode)				
Class 1 = 3.84 W	Class 2 = 6.49 W	Class 3 = 13.0 W	Class 4 = 25.5 W	Class 5 = 35.6 W (1)

(1) The relatively high power associated with Class 5 is made possible by a higher PSE minimum voltage (52 V) provided by Type 4 PSEs.

1.3. High-level operation

When a dual-signature PD is connected to a PSE, the general order of events on each pairset is as illustrated in Figure 4, which also highlights the various mechanisms that IEEE802.3 Power over Ethernet defines to prevent voltage from being applied unless a valid PD is connected. Connection Check and Detection, despite being distinct functions, are shown within the same block because the standard affords the implementer quite a bit of flexibility as to their sequencing.

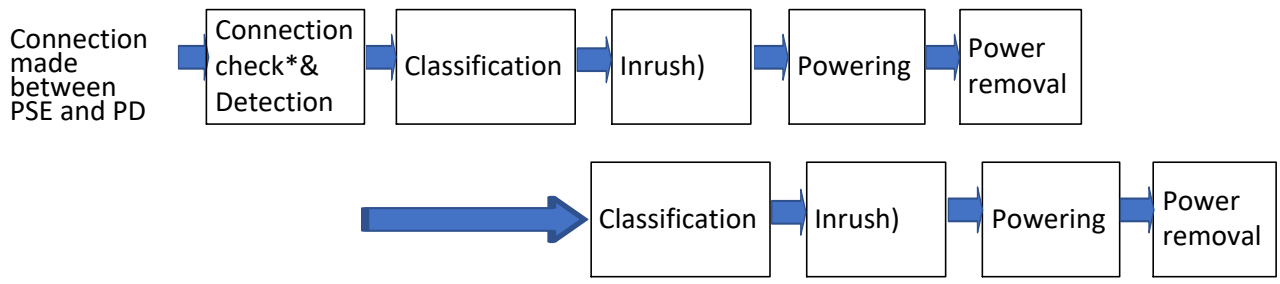

Figure 4: Typical startup procedure for a PSE operating with a dual-signature PD

In the state PSE state diagram, each Alternative serves a distinct role during 4-pair operation. In any implementation, the roles of the Alternatives are established in IDLE and are maintained in every other state. In the state diagram, the roles of the Alternatives are named Primary Alternative and Secondary Alternative.

Once an Alternative of the PSE is defined to be primary (can be Alternative A or Alternative B) and the PSE detects a dual-signature PD with a valid detection signature on the primary pairset, the PSE may continue to classification and power-up on that pairset. The secondary Alternative can then begin detection at any time after the primary's successful detection and may subsequently continue to classification and power-up. Alternatively, dual-signature PDs can be powered in parallel (i.e. detection, connection check, classification, and power-up may be done in parallel on both pairsets). Refer to the state diagram in the IEEE Std 802.3bt™-2018 standard for all permitted power-up sequences.

2. Detection

PSE: 145.2.6 PSE detection of PDs
PD: 145.3.4 PD valid and non-valid detection signatures

In general, dual-signature PD detection requirements are the same as those for single-signature PDs. The one difference of note is that a dual-signature PD must present a valid detection signature on each mode regardless of the voltage applied on the other mode. In single-signature PDs, there is a lone detection circuit, which results in an invalid signature on the unpowered pairset when the other pair is powered. On the other hand, with dual-signature PDs, it is possible that the first pairset will be powered while the other pairset is still performing detection, and that condition should not lead to a detection failure due to pollution of the signature by the powered pairset.

3. Connection check

PSE: 145.2.7 Connection check requirements
PD: 145.3.5 PD signature configurations

Connection check is the mechanism by which a 4-pair capable PSE probes the PI to distinguish a dual-signature PD from a single-signature PD or an invalid PD. In contrast, a 2-pair PSE cannot perform connection check, so it will not know if a connected PD is single- or dual-signature without additional identification information. Therefore, a 2-pair PSE will treat all PDs as if they were single-signature.

3.1. Dual-signature PD configuration

To identify a dual-signature PD, connection check relies on the PD's signature configuration, which is shown in Figure 5. The essence of a dual-signature PD is that each Mode is connected to an individual PD controller. As a result, the detection and classification mechanisms may return different results through Mode A and Mode B. Furthermore, even if Mode A is powered, it is still possible to perform detection and classification on Mode B, and vice versa.

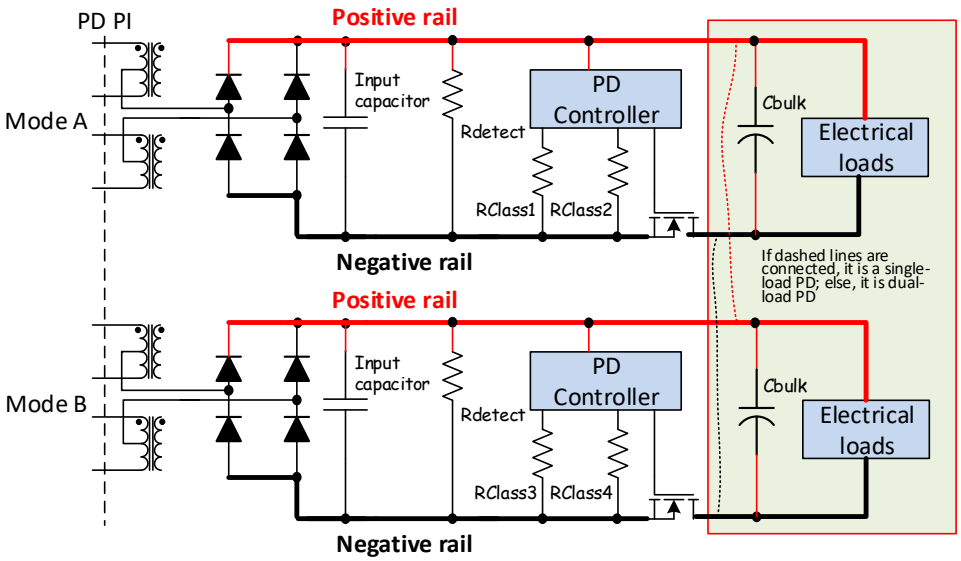

Figure 5: Conceptual diagram of a dual-signature PD

The standard specifies the dual-signature PD as if it has two internal, isolated PD loads encapsulated within a single PD entity connected to one PI. This concept simplifies significantly the specifications for dual-signature PDs in terms of detection, classification, power-up, power-on, current sharing, and current unbalance by specifying the requirements and sequence of operation for a Mode independently of the status of the other Mode.

The specific requirement that defines a "dual-signature PD" is as follows: "A dual-signature PD shall present a valid detection signature on a given Mode, regardless of any voltage between 0 V to 57 V applied to the other Mode." In short, the requirement is to present a valid signature on a Mode regardless of the voltage or current applied to the other Mode.

4. Classification

PSE: 145.2.8 PSE classification of PDs and mutual identification
PD: 145.3.6 PD classification
145.3.7 PSE Type identification

Classification of dual-signature PDs, while reliant on the same fundamental process of issuing class and mark events to determine the requested class and convey an assigned class, does differ from that of single-signature PDs in some ways. Perhaps most notably, each pairset must be independently classified prior to application of operating voltage on that pairset.

Another difference is in the relation between the PSE Type and the number of class events that can be produced for dual-signature PDs (see Table 5). Because the highest Class that can be assigned per pairset is Class 5, fewer class events need to be issued by the PSE for Type 3 and Type 4 dual-signature PDs relative to their single-signature counterparts.

Table 5: PSE Type and corresponding maximum number of class events and assigned Class

PSE Type	Maximum number of class events	Highest assigned Class for a pairset
1[1]	1	3
2[1]	2	4
3	3	4
4	4	5

Note 1: only one mode can be powered

Table 6 shows the class signature the PD produces for each class event and includes single-signature PDs to succinctly illustrate the differences from dual-signature PDs. A class signature denoted by "[]" indicates that this number of class events will not occur in a compliant system, as well as the resultant class signature if the PSE were to spuriously issue the additional class event(s).

Table 6: PD requested Class and corresponding class signatures

Requested Class	Class signature produced by the PD				
	Event 1	Event 2	Event 3	Event 4	Event 5
Single-signature PD					
Class 1	1	1	1	[1]	[1]
Class 2	2	2	2	[2]	[2]
Class 3	3	3	3	[3]	[3]
Class 4	4	4	4	[4]	[4]
Class 5	4	4	0	0	[0]
Class 6	4	4	1	1	[1]
Class 7	4	4	2	2	2
Class 8	4	4	3	3	3
Dual-signature PD					
Class 1	1	1	0	[0]	[0]
Class 2	2	2	0	[0]	[0]
Class 3	3	3	0	[0]	[0]
Class 4	4	4	0	[0]	[0]
Class 5	4	4	3	3	[3]

A Type 3 or Type 4 dual-signature PD changes its response between the second and third class events in order to indicate its Type and ability to accept 4-pair power to a Type 3 or Type 4 PSE. To a Type 1 or Type 2 PSE, a Class 5 PD will look like a Class 4 PD because the PSE will not produce the third class event, which the PD uses to signal its request for more than Class 4 by changing the class signature.

Table 7 shows how the assigned Class of a dual-signature PD is a function of its requested Class and the number of class events produced by the PSE. The derivation of the assigned class for a dual-signature PD is like that of a single-signature PD. While the PD is requesting power during classification, the PSE is allocating (i.e. granting) power. This is done through the number of class events that the PSE produces. The maximum possible class events for a PSE connected to a dual-signature PD is four (and five for single-signature PD).

Table 7: Derivation of assigned Class and power levels for a PSE and a dual-signature PD

Requested Class	Number of class events			
	1	2	3	4
Class 1	Class 1	Class 1	Class 1	X
Class 2	Class 2	Class 2	Class 2	X
Class 3	Class 3	Class 3	Class 3	X
Class 4	Class 3	Class 4	Class 4	X
Class 5	Class 3	Class 4	Class 4	Class 5

A PSE may not produce more class events than needed to satisfy the PD's requested power (e.g. a PSE capable of Class 5 power is not permitted to produce four class events when the PD only requests Class 3). However, a PSE may produce fewer class events than necessary to satisfy the PD's requested power, which indicates power demotion, as specified in the IEEE Std 802.3bt™-2018 standard. A green colored cell indicates that the assigned Class is equal to the requested Class, while a white cell indicates that the PD has been power demoted. A cell marked with a cross indicates that the PSE is not permitted to produce the corresponding number of class events.

Table 8 shows the resulting assigned Class based on the PD's requested Class and the number of class events that the PSE produced over each pairset. The orange entries highlight cases of power demotion, which refers to a PD being assigned less power than requested. Any dual-signature PD can be demoted to:

- Class 3 power if the PSE produces only one class event
- Class 4 power if the PSE only produces two or three class events

Power demotion allows a PSE to supply power to a PD even if the PSE does not have all of the PD's requested power available, allowing higher power PDs to operate in a feature-reduced mode when connected to lower power PSEs.

Table 8: Assigned Class and number of class events based on available PSE power and the PD's requested Class

PSE available power	Requested Class by the PD				
	Class 1	Class 2	Class 3	Class 4	Class 5
Class 1	Class 1 (1,2,3 EV)	No power	No power	No power	No power
Class 2	Class 1 (1,2,3 EV)	Class 2 (1,2,3 EV)	No power	No power	No power
Class 3	Class 1 (1,2,3 EV)	Class 2 (1,2,3 EV)	Class 3, (1,2,3 EV)	Class 3 (1 EV)	Class 3 (1 EV)
Class 4	Class 1 (1,2,3 EV)	Class 2 (1,2,3 EV)	Class 3, (1,2,3 EV)	Class 4 (2,3 EV)	Class 4 (2,3 EV)
Class 5	Class 1 (1,2,3 EV)	Class 2 (1,2,3 EV)	Class 3, (1,2,3 EV)	Class 4 (2,3 EV)	Class 5 (4 EV)

Together, Figure 6 and Figure 7 provide an example of a Type 4 PSE connected to a Type 4 dual-signature PD, which in this case has a different requested Class over each Mode. Specifically, the PD requests Class 5 over Mode A and Class 3 over Mode B.

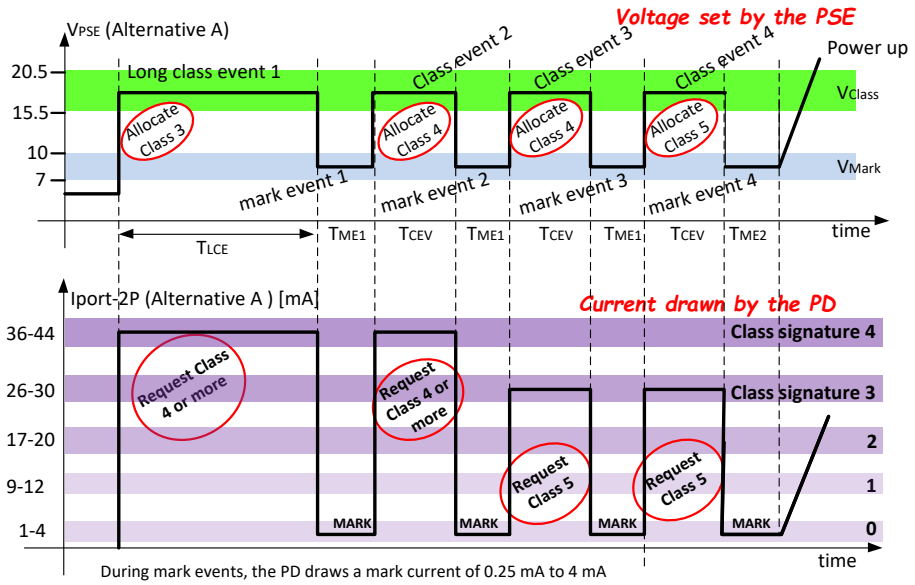

Figure 6: Physical Layer classification with Type 4 dual-signature PD with requested Class 5 on Mode A

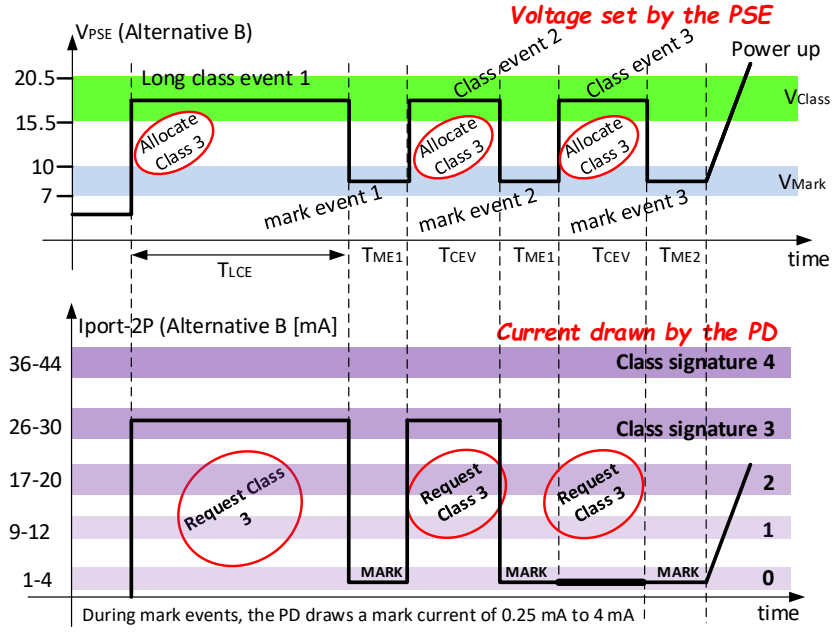

Figure 7: Physical Layer classification with Type 4 dual-signature PD with requested Class 3 on Mode B

4.1. Classification terminology

For dual-signature PDs, all the same classification terminology as for single-signature PDs applies, albeit per pairset.

4.2. Class probing

In addition to discovering the requested Class of a PD, a Type 3 or Type 4 PSE can use class probing to collect 4PID information for dual-signature PDs. This is done by generating at least three class events to determine if the dual-signature PD is 4-pair capable and above Class 4 for each pairset. A class reset is required afterward to reset the PD's classification state machine.

4.3. Mutual identification

While the mutual identification mechanism has a few blind spots for both single-signature and dual-signature PDs, Type 3 and Type 4 dual-signature PDs do have different class signatures for each requested Class, starting from the 3rd class event eliminating any blind spots for Type 3 and Type 4 PSEs. In contrast, for single-signature PDs that request Class 4 and below, it is not possible for the PSE to determine if it's a Type 3 PD or a Type 1 / Type 2 PD because the class responses are identical.

The PSE can discover the PD's Type based on the requested Class of the dual-signature PD, as shown in Table 9. The results for single-signature PDs are included to emphasize their additional ambiguity.

Table 9: Deriving PD Type from the requested Class

Requested Class	PD Type
Single-signature PD	
0	Type 1
1, 2, or 3	Type 1 or Type 3
4	Type 2 or Type 3
5 or 6	Type 3
7 or 8	Type 4
Dual-signature PD	
1, 2, 3, 4	Type 3
5	Type 4

4.4. DLL classification

79.3.2 Power via MDI TLV
145.5 Data Link Layer classification

Data Link Layer (DLL) classification is equally applicable to single-signature and dual-signature PDs, as is the requirement that PDs are not allowed to request more power through DLL than they requested through Physical Layer classification. The main difference between a single-signature PD and a dual-signature PD in regard to DLL classification is that power negotiation occurs per Mode for dual-signature PDs rather than as a sum, as with single-signature PDs. In other words, for a single-signature PD, the allocated power and requested power are the total power of both pairsets when the power is theoretically split evenly between the two pairsets (ignoring the effect of pair to pair unbalance). On the other hand, for dual-signature PDs, the allocated power to the PD is done per pairset and is specified as PClass_PD-2P which is more restrictive than single-signature PD as explained in section 7.1.

As an example, a dual-signature Class 5 PD that requests 35.6 W through Physical Layer classification over Mode A can use DLL classification to lower its request to 28 W, allowing the PSE to recover part of the allocated power for this Mode. As another example, a dual-signature Class 5 PD that was assigned to Class 4 (power demotion) can use DLL to request Class 5 power again (if the reason the PSE assigned the PD to Class 4 was due to a lack of available power, it may later be able to reclassify the PD as Class 5 and allocate its full requested power).

For dual-signature PDs, four fields in the Power over Ethernet TLV are used to negotiate a new power allocation between a PSE and a PD: the 'PD requested power value Mode A' field, 'PD requested power value Mode B' field, 'PSE allocated power Alternative A' field, and the 'PSE allocated power Alternative B' field. These four fields are 4 bytes each and are interpreted as an

unsigned integer number. These fields allow power negotiation per each Mode separately. In order to simplify the text and the state machines, the standard use the notation of 'Mode (X)' or 'alt (X) for example: PSEAllocatedPowerValue_alt(X) or PDRequestedPowerValue_Mode(X), where X=A or B.

When a dual-signature PD is connected to a PSE, the fields for single-signature PDs are set as follows:
When a PSE, connected to a dual-signature PD, transitions from 4-pair to 2-pair operation, it assigns the value of PSEAllocatedPowerValue_alt(X), where X is the powered Alternative, to PSEAllocatedPower- Value. The purpose of this is that the PD can continue operating over the remaining powered Mode.
When a PSE, connected to a dual-signature PD, transitions from 2-pair to 4-pair operation, it assigns the value of PSEAllocatedPowerValue to PSEAllocatedPowerValue_alt(X), where X is the Alternative that was initially powered.
A dual-signature PD that is switched from 4-pair to 2-pair mode requests the amount of power it needs for 2- pair operation in the PDRequestedPowerValue variable which is the requested power for the powered Mode.

In addition, the ‘PSE maximum available power value’ field contains the highest power the PSE can grant and may be used for both single-signature and dual-signature PDs. The PSE sets the value of this field taking available power budget and hardware capabilities into account. When connected to a dual-signature PD, this value refers to the total amount of power available at the PI, even though power is allocated separately on a per pairset basis.

A PD can request power by putting the amount of power it needs in the ‘PD requested power value Mode (X)’ field and sending an updated LLDP frame. The value represents a power level in $1/10^{th}$ of a Watt increments (e.g. value 255 represents 25.5 W). The PSE, upon reception, will evaluate the power request, and update the allocation. It will send the new power allocation in the ‘PSE allocated power value Mode (X)’ field. Only once the PSE and PD are in sync with each other, the power allocation changes. Beware that correct implementation of DLL requires more than this short description!

After a DLL transaction is successfully completed, both the allocated power (PSEAllocatedPowerValue_Mode(X)), and the PD power limit (PDMaxPowerValue_Mode(X)) will be set to the new negotiated power level. As a result, it is possible that the assigned Class changes! For example, a PD that requests Class 5 but gets power demoted to Class 4 will initially start with PSEAllocatedPowerValue_Mode(X) and PDMaxPowerValue_Mode(X) at a value of 255 (representing Class 4 power limit of 25.5 W). Later on, the PD requests what it really needs (35.6 W), and this is granted by the PSE, provided that it is able to allocate the requested amount of power. Now PSEAllocatedPowerValue_Mode(X) and PDMaxPowerValue_Mode(X) are both equal to 356. The PD has now been re-assigned to Class 5, which means that all the class dependent requirements may have changed. A mapping between the values of PSEAllocatedPowerValue_Mode(X) and PDMaxPowerValue_Mode(X) and the resulting assigned Class are listed in Table 10.

Table 10: Relation between negotiated DLL power and the assigned Class

PSEAllocatedPowerValue (PSE) PDMaxPowerValue (PD)	Assigned Class	PSEAllocatedPowerValue_alt(X) (PSE) PDMaxPowerValue_mode(X) (PD)	Assigned Class
Single-signature PD		Dual-signature PD	
1 – 39	Class 1	1 – 39	Class 1
40 – 65	Class 2	40 – 65	Class 2
66 – 130	Class 3	66 – 130	Class 3
131 – 255	Class 4	131 – 255	Class 4
256 – 400[1]	Class 5	**256 – 356[1]**	Class 5
401 – 510	Class 6	NA	NA
511 – 620	Class 7	NA	NA
621 – 999	Class 8	NA	NA

Note 1: The differences for assigned Class 5 between single-signature PD and dual-signature PD are resulting from the following: in single-signature PD the maximum Class is 8 and for Class 5 the maximum power a PD may draw over 4-pairs is 40 W while in dual-signature PD the maximum Class is 5 and for Class 5 the maximum power a PD may draw over a pairset is 71.3 W/2=35.65 W rounded by the standard to 35.6 W per pairset.

5. Autoclass

Autoclass is not specified for dual-signature PDs.

6. Inrush

PSE: 145.2.10.7 Current during power up
PD: 145.3.8.3 Input inrush current

Inrush is the last phase before operating power is applied and the system begins normal operation over each pairset. Regardless of PD configuration, inrush is the controlled application of power, to gently switch over from a non-powered state to a powered state. A large portion of interoperability problems stem from PD implementations that do not correctly implement inrush. Designers are encouraged to carefully read this section, as well as the relevant sections on inrush in the 802.3bt standard.

The inrush phase behavior for a PSE when connected to a dual-signature PD is similar to the case with a single-signature PD. However, there are some differences, which are described in Table 11.

Table 11: Inrush differences between dual-signature and single-signature PDs

	Single-signature PD	Dual-signature PD
	The inrush phase is specified for all pairsets and per pairset by Iinrush and Iinrush-2P, respectively, for the PSE, and Iinrush-PD and Iinrush-PD-2P, respectively, for the PD.	The inrush phase is specified per pairset: Iinrush-2P for the PSE, and Iinrush-PD-2P for the PD. The total current is not pertinent and hence not specified.
	Iinrush, Iinrush-2P, Iinrush-PD, and Iinrush_PD-2P are functions of the assigned class.	Iinrush-2P and Iinrush_PD-2P are the same for all classes.
	The inrush current is measured for compliance at the negative pairs per pairset and for the total current.	The inrush current is measured for compliance at the negative pairs per pairset.

As a brief aside, in most PSEs the positive pairs are tied together, which can theoretically result in high pair to pair unbalance on the positive pairs when connected to either a single-signature PD or a dual-signature PD with a single load. As a result, the per pairset unbalance behavior will be similar to a single-signature PD.

6.1. PSE inrush

After classification, if the PSE decides to apply power to the PD, it will first go through the Inrush phase. During inrush the PSE limits the amount of current being delivered to $I_{inrush-2P}$ for at least 50 ms and up to 75 ms for each pairset. $I_{inrush-2P}$ for a dual-signature PD is limited to 0.45 A for all classes . As shown in Figure 8, the minimum $I_{inrush-2P}$ is a function of the voltage on the PSE PI.

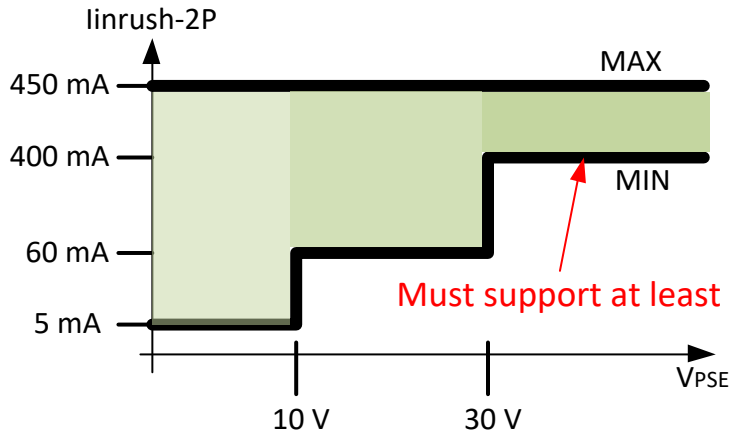

Figure 8: PSE inrush current per pairset for a dual-signature PD, $I_{inrush-2P}$

During the first 50 ms of the inrush phase, the PSE limits the inrush current to a current of IInrush-2P over each pairset. The values of the input current are not dependent on the assigned Class, but rather the voltage at the PSE PI. During the “PSE inrush” phase there is no particular requirement on the PD.

In order to decrease the thermal load on the PSE current limiter, the full inrush current is only required when the voltage has risen above 30 V.

6.2. Dual-signature PD inrush

For a dual-signature PD, the inrush phase begins when the PD voltage (VPD) over a pairset exceeds the PD turn on voltage (VOn_PD), which is anywhere in the range of 30 V to 42 V. This moment is named t0. The inrush phase ends 80 ms after t0. All of these timing parameters are summarized in Figure 9.

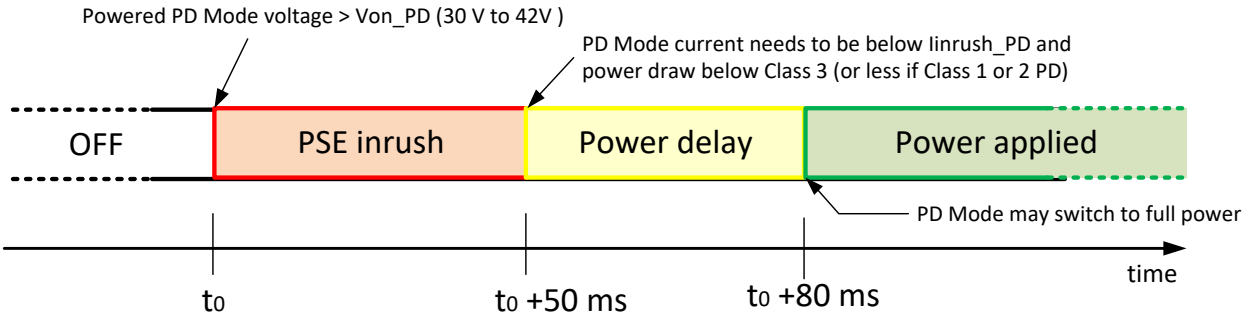

Figure 9: Dual-signature PD inrush time phases per pairset

For dual-signature PDs, the inrush process is performed for each pairset independently from the other pairset. In contrast, for a single-signature PD, the inrush process is done over 4-pairs in a timeframe of 75 ms for all 4 pairs.

After 50 ms, the PD is in the power delay phase, which lasts for 30 ms. Somewhere in the PD power delay phase, the PSE switches from its inrush state, to its powering state. During this time, a dual-signature PD needs to meet the following requirements:

1. Have a pairset **current** less than IInrush-2P.
2. Have an input **power** less than Class 3 (13 W) or the PD's requested Class, whichever is lower, over each pairset.

The reason for item 2 above is that the PSE can switch out of inrush at any time between 50 ms to 75 ms and immediately enforce the assigned Class.

To meet these requirements, it is highly recommended to keep the PD electrical load disabled until the PD is solidly into the 'power applied' state. If the load is turned on prematurely, part (or all) of the current the PSE provides is taken by that load and prevents the bulk capacitor from charging.

There are several methods employed by dual-signature PDs to complete inrush:

1. The PD does not perform any form of inrush control. Once the PSE turns on and the PD voltage has risen above VOn_PD, the PD's power switch turns on and stays on. This has the effect that the voltage at the PD PI (and PSE PI) collapses to near zero. As can be seen in Figure 9, PSEs are allowed to deliver small currents at this voltage. Unless the PSE provides significantly more inrush current than the minimum required by the standard or the PD has sufficiently low bulk capacitance, inrush will fail because the bulk capacitor of the PD will not be charged when the PSE transitions from inrush to power on. Such a PD fails to comply with the VOff_PD requirement, which states that below 30 V a PD must be "turned off".

2. The PD does not perform inrush current limiting but adheres to the VOn_PD/ VOff_PD requirement. Whenever the PD turns on, it will transfer the charge in its small input capacitor (maximum 120 nF in addition to PSE output capacitance, which is maximum 0.52 uF) through the power switch to its larger bulk capacitor. Once the voltage is reduced to VOff_PD, the power switch turns off. This will cause the power switch to rapidly turn on and off, essentially acting as a switched-capacitor current regulator. Besides being inefficient, such a PD violates the requirement that a PD may not oscillate during turn on.

3. The PD limits the inrush current below IInrush_PD-2P. Once the PD turns on, it limits the inrush current to a value below IInrush_PD-2P (400 mA per pairset). The voltage at the PD and PSE PI does not collapse, but quickly rises to the nominal operating voltage. Because the PD controls the inrush current, its power switch carries the thermal load of inrush rather than the PSE. The PD maintains the current control until the bulk capacitor is charged. PDs that use this method meet the inrush requirements regardless of bulk capacitor size and PSE inrush current levels.

Note that at t0 + 50 ms, in addition to drawing less than IInrush_PD-2P, the PD must conform to the power limits of the "Power delay" state. This power limit is 13 W if the PD requested Class 3 or higher, or 3.84 W or 6.49 W if the PD requested Class 1 or Class 2, respectively. The corresponding input current limits are significantly below the IInrush_PD-2P value. After the power delay state, the PD has reached the nominal operating phase and can draw power up to the assigned Class.

7. Operating power

PSE: 145.2.8 PSE classification of PDs and mutual identification
145.2.10 Power supply output
145.2.11 Power supply allocation
PD: 145.3.6 PD classification
145.3.8 PD power
145.3.8.2 Input average power

Following successful detection and classification, a system enters the nominal powering state, where it spends most of its time. During this time, the PSE checks for abnormal conditions on each pairset, like overloads or short-circuits, as well as checking that the PD remains connected. As a result of classification, the PD will either have been assigned to the Class it requested or have been power demoted. In either case, both the PSE and the PD are required to conform to the requirements of the assigned Class per pairset.

In the powering state, a single-signature PD is powered as a single-load device, where each pairset is monitored for overload or short circuit independently, and the PSE continually checks that the PD remains connected. A dual-signature PD is powered per pairset independently (regardless if it is a dual-signature PD with as single load or dual load) where .each pairset is monitored for overload and short circuit, and the PSE continually checking that each PD mode remains connected.

7.1. Dual-signature PD power limits

There are two possible power limits that may apply to a PD. Table 12 indicates under which conditions the various power limits apply.

1. **PClass_PD-2P** is the maximum amount of input average power for a given Class at the PD PI over each pairset for a dual-signature PD. When a PD is powered and has not performed DLL classification, the power limit for the PD is PClass_PD-2P for the assigned Class.

2. **PDMaxPowerValue_mode(X)** is a maximum power value expressed in 1/10th of a Watt. This value is the result from Data Link Layer Classification, which allows the PSE and dual-signature PD to negotiate the amount of allocated power over Mode (X). After a successful DLL negotiation, PDMaxPowerValue_mode(X) is the applicable limit. The corresponding PDMaxPowerValue_mode(X) is lower than or equal to PClass_PD-2P.

Table 12: Applicable power limits for a dual-signature PD

Condition	Applicable limit
Power applied after classification for dual-signature PD	PClass_PD-2P
After the successful conclusion of a DLL power negotiation over Mode (X)	PDMaxPowerValue_mode(X)

The dual-signature PD needs to take several requirements on input power into account:

- There is a limit on peak power that it is not allowed to exceed. In the standard, this is referred to as $P_{Peak\_PD\text{-}2P}$, and the value depends on the assigned Class, as shown in Table 13.
- Within a 1 second sliding window, the PD may exceed $P_{Class\_PD\text{-}2P}$ or PDMaxPowerValue_mode(X) (whichever is applicable), for up to 50 ms, up to $P_{Peak\_PD\text{-}2P}$.

- The average input power over a 1 second sliding window may not exceed P_{Class_PD}-2P or PDMaxPowerValue_mode(X) (whichever is applicable). This includes any peak power that is drawn inside of that window. An example is shown in Figure 10, where the average power of f(t) over 1sec is less or equal to PClass_PD_PD or PDMaxPowerValue-2P.

Table 13: Power levels for PSE and dual-signature PD as a function of assigned Class

	PD limits		PSE highest nominal power	
Assigned Class	PClass_PD-2P (W)	Ppeak_PD-2P (W)	PClass-2P[1] (W)	Ppeak-2P[1] (W)
1	3.84	5	4	5.13
2	6.49	8.36	6.7	8.74
3	13	14.4	14	15.62
4	25.5	28.3	30	34.12
5	35.65	37.43	45	48.1

Note 1: Worst-case value based on using Equation 145-3 for dual-signature PD under the following conditions: Dual-signature PD Class 1 to Class 4: PSE voltage 50 V and Rchan=12.5 Ω. Dual-signature PD Class 5: PSE voltage 52 V and Rchan=12.5 Ω

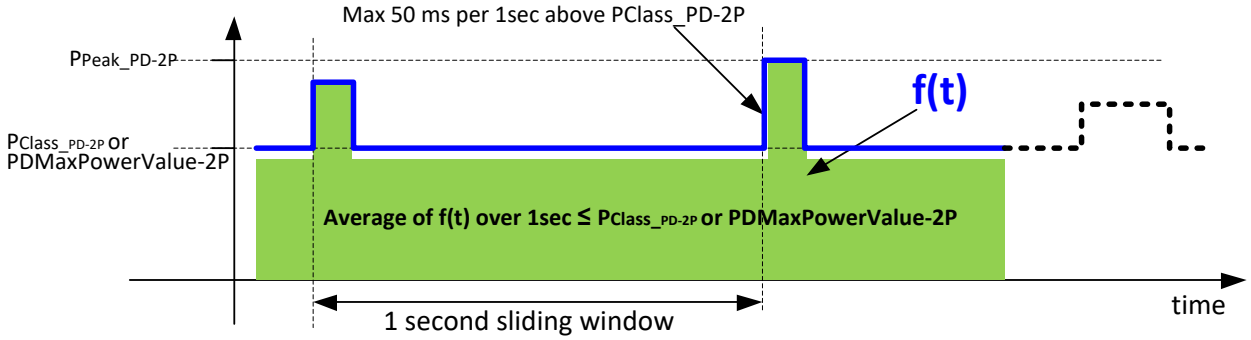

Figure 10: PD input average power and peak power for single-signature and dual-signature PD

The PSE's powering sequence for a dual-signature PD is noteworthy. Unlike in the single-signature PD case where, when operating over 4 pairs, the second pairset must be turned on within 75ms of when the first pairset is turned on, a PSE connected to dual-signature PD may do detection and classification in parallel and turn on both pairsets simultaneously, or it may perform detection, classification, and power-up with any powering time delay limit between the two pairsets. The latter requires the dual-signature PD with a single-load to be carefully designed to ensure that the PD will not enter an overload condition when only one pairset is powered.

Figure 11 demonstrates two main use cases:

a) Parallel operation with no power sequence delay between the pairsets.

b) Long power sequence delay time. The power sequence delay *can be from close to zero up to any value*. In addition, Figure 11 shows that the limits of the power and current values over each pairset shall not exceed $P_{Class\text{-}PD\text{-}2P}$, $I_{Con\_PD\text{-}2P}$, and $I_{Peak\_PD\text{-}2P}$ in order for the PD to be compliant.

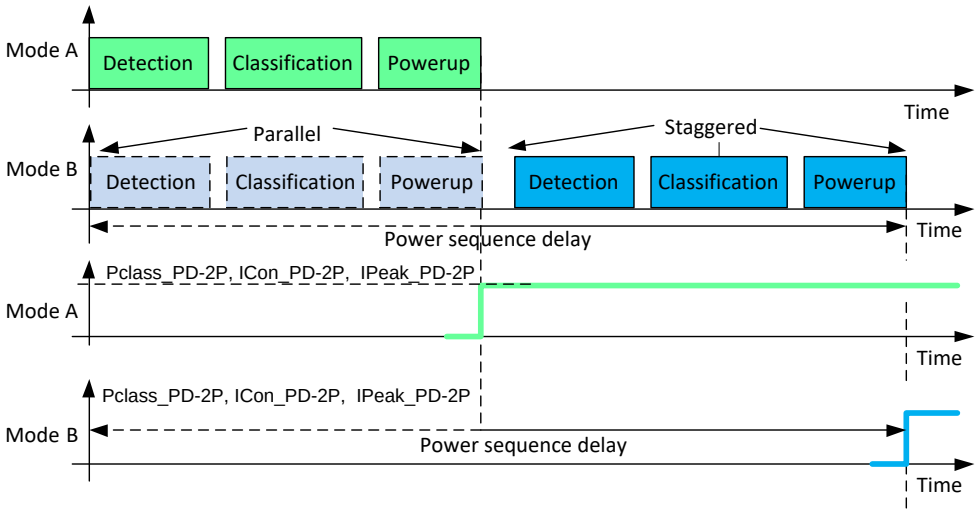

Figure 11: Dual-signature power sequence delay range

Dual-signature PDs that are dual-load are typically less sensitive to power sequence time delay since their detection, classification, DC/DC converters, and loads over each pairset are completely isolated from each other. However, the sensitivity to power sequence time delay is application dependent (i.e. is the powering of one of the modes (A or B) critical to the operation of the other mode (B or A)?).

It is recommended that a dual-signature PD that is single-load advertise the same class on each pairset due to the fact that, eventually, it will share the input power, resulting in the power consumed by the PD being divided almost equally between the Modes (ignoring the unbalance effect), as with a single-signature PD. As explained earlier, the standard specifies more restrictive unbalance requirements for single-load dual-signature PDs by limiting the power consumed over each pairset to the assigned class, $P_{Class\_PD\text{-}2P,}$ and the current flow through each Mode to not exceed $I_{Con\_PD\text{-}2P}$ and $I_{Peak\_PD\text{-}2P}$. This approach significantly simplified the standard for dual-signature PDs.

7.2. PSE power when connected to a dual-signature PD

145.2.10.6 Continuous current capability in the power on states
145.2.10.8 Overload current
145.2.10.9 Short circuit current

Most of the dual-signature specifications in Clause 145 are in relation to current on a per pairset basis (e.g. Icon-2P, Ipeak-2P, Icut-2P, ILIM-2P, etc.). Therefore, the PSE operating current templates (see Figure 12 and Figure 13) are specified per pairset for dual-signature PDs.

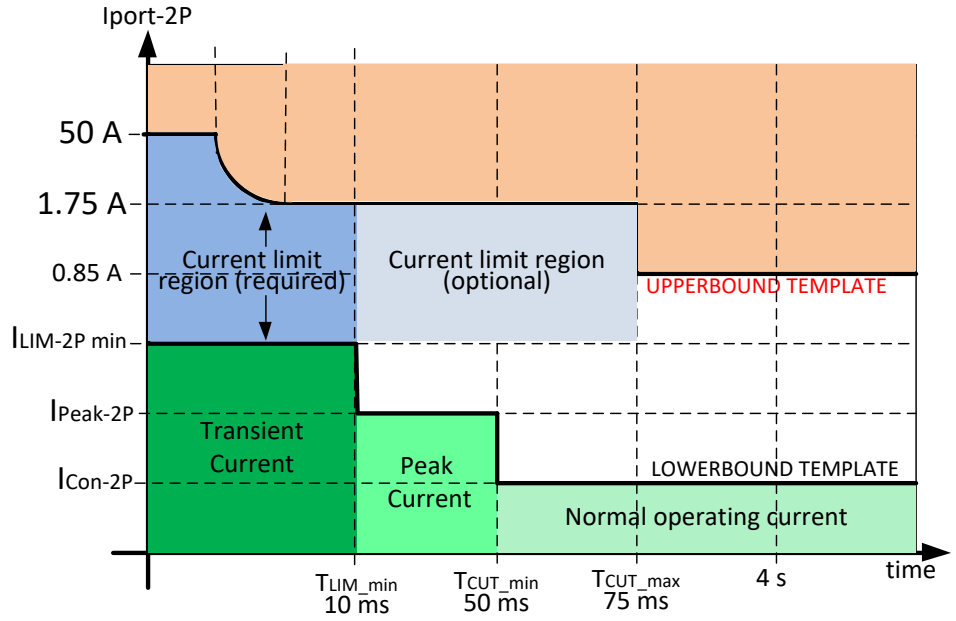

Figure 12: Type 3 PSE operating current template

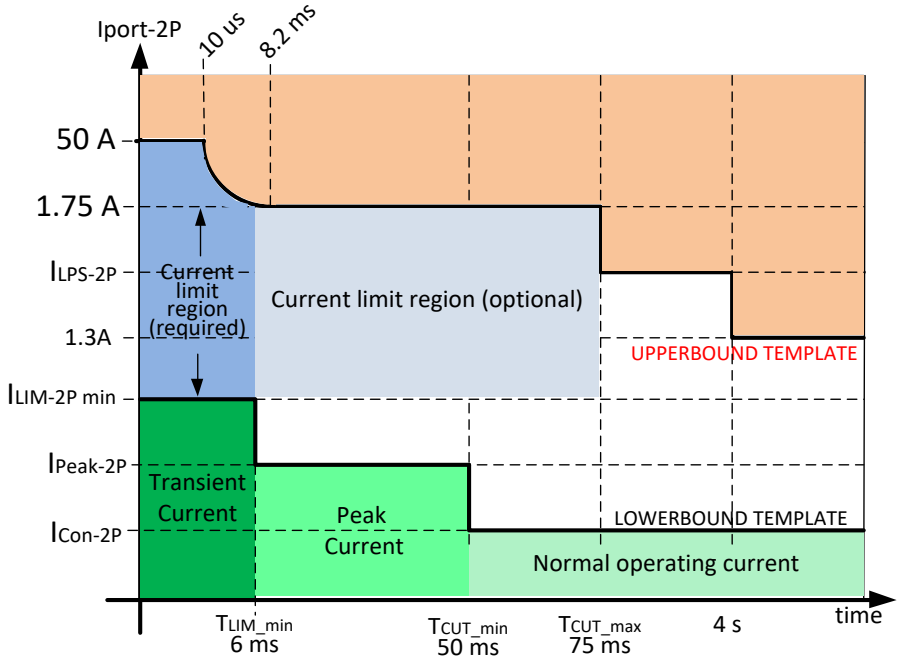

Figure 13: Type 4 PSE operating current template

The lowerbound template for the 'normal operating current' region (the rightmost region) has a value of I_{Con-2P}, the operating current the PSE supports indefinitely. When the PSE is powering the PD over a pairset, I_{Con-2P} is defined as follows:

$$I_{con-2P} = P_{Class-2P} / V_{PSE} \quad (1)$$

I_{Con-2P} The current the PSE supports on a pairset indefinitely

$P_{Class-2P}$ The amount of output power required to supply P_{Class_PD-2P} at the PD PI, given a certain cable resistance ($R_{Chan-2P}$) and the actual PSE voltage (V_{PSE})

VPSE The actual PSE PI voltage

Finally, PClass-2P, the amount of power the PSE needs to support to provide PClass_PD-2P at the PD PI, is defined as:

$$P_{Class-2P} = V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE} - 4 \times R_{Chan-2P} \times P_{Class\_PD-2P}}}{2 \times R_{Chan-2P}} \right) \quad (2)$$

PClass-2P The amount of output power required to supply PClass_PD-2P at the PD PI, given a certain cable resistance (RChan-2P) and the actual PSE voltage (VPSE)
VPSE The actual PSE PI voltage
RChan-2P The actual loop resistance between the PSE and the PD
PClass_PD-2P The maximum average amount of power a PD may draw for a particular assigned Class over a pairset

Because the PClass-2P equation depends on the **actual** cable resistance (not the worst-case) and the actual PSE output voltage, this allows the PSE to optimize the power it budgets for the PD. The next segment to the left of the lowerbound template serves to allow a PD to draw peak power. The requirements for peak current are identical to those of the normal operating current, with the exception that PPeak-2P is determined using PPeak_PD-2P. A PSE must support this output current for at least TCUT min (50 ms) in any 1 second window.

The final segment (leftmost) of the lowerbound template is the transient current. For a duration of at least TLIM-2P min, the PSE is required to actively limit the output current to any value between ILIM-2P and the upperbound template. For a Type 3 PSE this timer period is 10 ms, while for a Type 4 PSE it is 6 ms. Therefore, during this time it is impossible for a PD to violate the upperbound template.

The upperbound template is identical to single-signature PD.

7.3. PSE current limiting

145.2.10.3 Voltage transients
145.2.10.9 Short circuit current

The requirements for limiting the current for dual-signature PDs are similar to those required for single-signature PDs. The requirements are specified over each pairset for single-signature and dual-signature PDs.

7.4. Powering configurations

PSE: 145.2.4 PSE PI
PD: 145.3.2 PD PI

Since dual-signature PD operation is defined per pairset, switching between 2-pair and 4-pair and vice versa (for classes 1 to 4) is not a relevant feature since normal operation with a dual-signature

PD is based on an end goal of 4-pair operation for any class. However, it is possible that after a fault, the faulty pairset will be turned off and power will continue to be supplied to the other pairset.

See Table 14 for an overview of what options exist pertaining to 2-pair and 4-pair power for the different PSE Types and assigned Classes.

In order to assign class 5, the Type 4 PSE must be operating in 4-pair mode.

Table 14: 2-pair and 4-pair powering rules for dual-signature PD

PSE Type	Assigned Class				
	1	2	3	4	5
1	2P	2P	2P		
2	2P	2P	2P	2P	
3	2P/4P	2P/4P	2P/4P	2P/4P	
4	2P/4P	2P/4P	2P/4P	2P/4P	4P

7.5. PD reflected voltage

PSE: 145.2.10.4 Reflected voltage
PD: 145.3.8.8 Reflected voltage

Reflected voltage (Vrefl) is a new term in IEEE Std 802.3bt™-2018. This parameter was referred to as backfeed voltage in Clause 33 (IEEE802.3af and IEEE802.3at standards) for Type 1 and Type 2 systems. In addition, the term 'reverse current' (Irev) was introduced in IEEE Std 802.3bt™-2018 to address more complex situations together with the 'reflected voltage'.

For dual-signature PDs, the requirements for reflected voltage are simpler yet more restrictive compared to single-signature PDs. When any voltage in the range of 0 V to 57 V max is applied per any of the valid PSE 2-pair configurations (see Figure 14 where it is a 2-pair PSE and Figure 15 where it is 4-pair PSE operating over 3-pair), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed 2.8 V. In contrast, for single-signature PD, Vrefl may be higher than 2.8V for VPort_PD-2P >10.1 V up to VPort_PD-2P max.

The rationale behind the requirement to limit the reflected voltage in any of the valid 2-pair configurations for dual-signature PDs was to prevent pollution of the detection circuit of the unpowered Mode in order to enable the other important requirement of a dual-signature PD to present a valid detection signature over each pairset regardless of the voltage applied to the other pairset.

To achieve the 2.8 V limit for reflected voltage is not an issue when typical diode bridges are used. When using ideal diode bridges i.e. when diodes are replaced with e.g. MOSFETs and a control circuit to operate them, some of these circuits in the market generate higher than 2.8V at the unpowered pairset when they operate in 3-pair mode.
In IEEE Std 802.3bt™-2018, for backwards compatibility considerations, the PD needs to meet this requirement when connected to a Type 1 or Type 2 PSE.

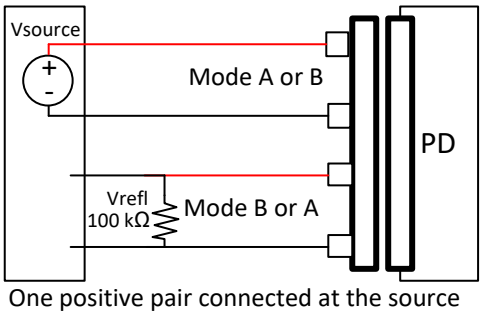

Figure 14: 2-pair operating power configuration

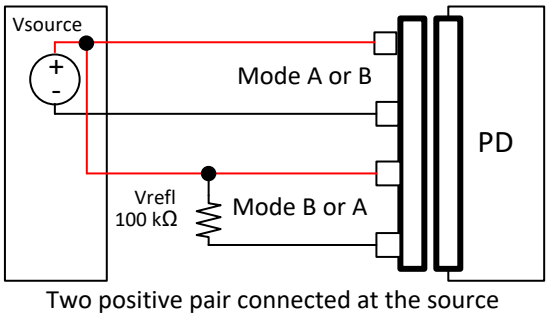

Figure 15: 3-pair operating power configuration

7.6. PSE reverse current

Dual-signature PDs are required to not generate reflected voltage (V_{REFL}) higher than 2.8V on the unpowered pairset when connected to 100 KΩ load which makes I_{REV} specification not relevant to PSE when connected to dual-signature PD.

8. Current unbalance in dual-signature PDs

PSE: 145.2.10.6.1 PSE pair-to-pair current unbalance
PD: 145.3.8.9 PD pair-to-pair current unbalance
See Annex 145A for more unbalance information

The unbalance requirements for a dual-signature PD are specified differently and are more restrictive than for a single-signature PD. Meeting dual-signature PD current unbalance requires the PD to not exceed Pclass-2P at the PSE PI over each pairset. As a result, even if pair to pair unbalance could occur with a single-load dual-signature PD, the unbalance effect is subject to ICon_PD-2P and IPeak_PD-2P.

Figure 16 shows a schematic of pair-to-pair current unbalance for a single-load dual-signature PD, which is identical for a single-signature PD. As a result, the pair to pair unbalance behavior of the dual-signature PD with a single-load is the same as in a single-signature PD.

In a single-load dual-signature PD, due to the existence of unbalance, the total PD load has to be reduced in order to keep both pairsets at or below PClass-PD-2P, which results in a slightly lower power utilization than a dual-load dual-signature or single-signature PD. The unbalance requirement over each pairset is to not exceed Icon-2P= (PClass-PD-2P / Vpd). In order to use all of the available power, such a PD would need to achieve perfect balance.

On the other hand, dual-load dual-signature PDs, given their isolation between pairs of the same polarity, don't have pair to pair unbalance issues (see Figure 17). Therefore, the requirement not to exceed, Icon-2P= (PClass-PD-2P / Vpd), is guaranteed by design (due to isolated loads) if PClass-PD-2P is met over each pairset.

The PSE is tested for unbalance compliance with a test verification model that represents a worst-case unbalanced PD configuration (which is the unbalanced single-signature PD and unbalanced link test verification model). If the PSE passes the PSE unbalance requirement, the PD passes the PD unbalance requirement, and a compliant cable is used, the resulting system has pair currents below those shown in Table 15 for single-signature PD or below PClass_PD-2P / VPD for dual-signature PD.

Measurement of Iunbalance-2P of a PSE is performed by connecting it to a test verification model that represents the load which consists of the worst-case unbalanced link and PD PI elements.
For the PD, measuring Iunbalance-2P is done by connecting the PD to a test verification model that represents a voltage source with its source resistance, which consists of the worst-case unbalanced link and PSE internal PI elements.

The test verification models are based on system worst-case unbalance equations that contain the contribution of the PSE, PD, and link to the system unbalance (For the dual-signature PD, Icon-2P is tested for compliance with the same test verification model used to test single-signature PDs for unbalance. The PSE is tested to meet $I_{Unbalance-2P}$ with the same test verification model for single-signature PDs).

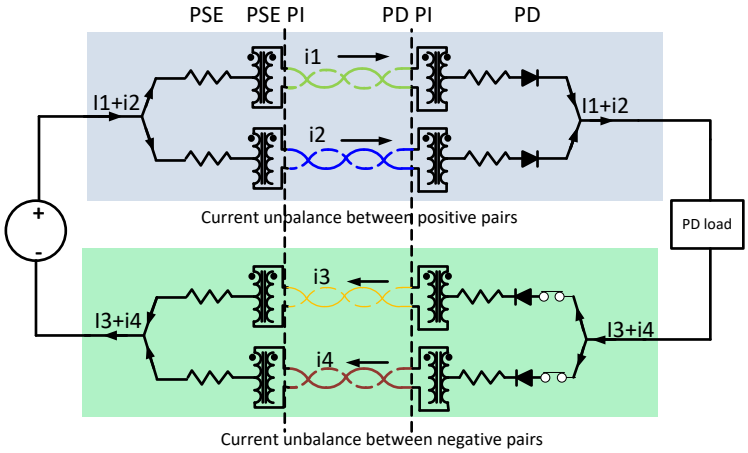

Figure 16: Overview of pair-to-pair current unbalance with a single-load dual-signature PD

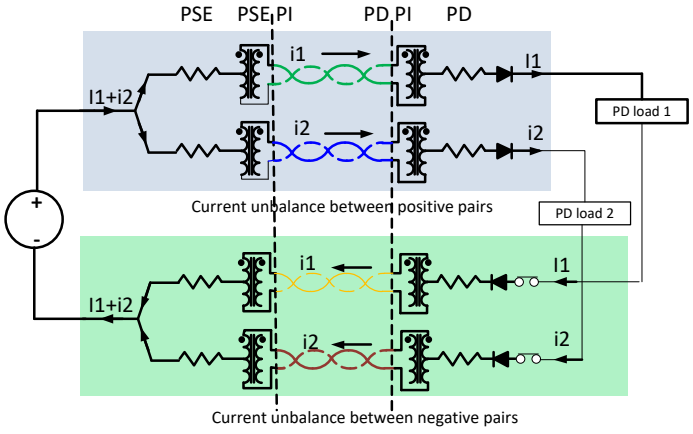

Figure 17: Overview of the lack of pair-to-pair current unbalance for a dual-load dual-signature PD

8.1. Dual-signature PD current unbalance

Unlike the PSE's verification circuit, the PD's unbalance verification circuit is defined over a continuous range of resistances. PDs that use diodes for rectification generally have the highest amount of current unbalance, resulting *from the forward voltage differences between the diodes on each pair of the same polarity* and the non-linear way diodes behave when conducting current in parallel. Because of this, PD designers should not assume that the worst-case unbalance occurs at the highest source resistance, but rather test for a suitable number of points in the source resistance range. In order to meet PD current unbalance requirements, it is recommended to control diode voltage difference to be less than 60mV (when measured at 10mA).

The above has much more importance in dual-signature PDs due to the fact that the PD must not exceed (PClass_PD-2P / VPD) over any pair, which leaves zero unbalance margin for single-load dual-signature PDs, meaning that the PD designer needs to ensure a bit lower power than PClass_PD-2P over each pairset or use current balancing techniques. On the other hand, dual-load dual-signature PDs don't have this challenge due to having practically zero unbalance.

9. Maintain Power Signature (MPS)

PSE: 145.2.10 PSE Maintain Power Signature (MPS) requirements
PD: 145.3.9 PD Maintain Power Signature

The minimum current a dual-signature PD must draw to avoid being disconnected by the PSE is called IPort_MPS-2P and is 10mA per pairset (i.e. each pairset is monitored independently for presence or absence of the MPS current). Many PDs will have a continuous current draw higher than IPort_MPS-2P.

The minimum MPS consists of a pulsed current, where its amplitude for a dual-signature PD is independent of the assigned Class of the PD. The on time and off time are dependent upon the Type of the PSE to which the PD is connected. Type 1 and Type 2 PDs are required to produce a minimum pulse of 10 mA for at least 75 ms with no more than 250 ms between the pulses. This translates to a power consumption of 54 V x 10 mA x 75 ms / (75 ms+250ms)=124.6 mW from the PSE, assuming the operating voltage is 54 V. A PD connected to a Type 1 or Type 2 PSE is also required to support ***another*** **form** of MPS measurements named "AC MPS". This involves presenting an impedance of no more than 26.3 kΩ continuously at the PD, consuming another 110 mW and resulting in a total power of 234.6 mW.

To further reduce minimum standby power consumption for PoE systems, Type 3 and Type 4 dual-signature PDs can make use of optimized MPS timings when connected to a Type 3 or Type 4 PSE, as shown in Figure 19. PDs assigned to Class 1 through 5 must draw a current of 10 mA for at least 7 ms with no more than 310 ms between pulses. This translates to an average power consumption of 12 mW per pairset, or about 1/10th (12 mW/ 124.6 mW) of the Type 1 / Type 2 minimum pulse average power consumption. If the PD is connected to Type 1 or Type 2 PSE which has to support AC MPS, we get a ratio of about 1/20th (12 mW/ (124.6 mW + 110 mW).

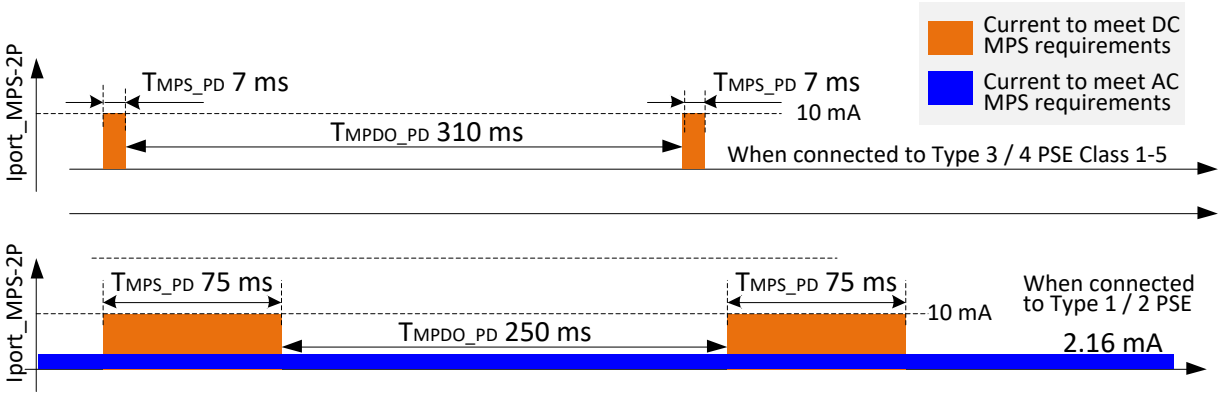

Figure 18: PD MPS requirements for a dual-signature PD

In dual-signature PDs, the MPS power consumption for both pairsets is 2 x (54 x 10 mA x 7 ms) / (7 ms + 310 ms) = ~24 mW. See Table 15 for PD MPS requirements as a function of PSE Type.

Table 15: PD MPS requirements and power consumption for dual-signature PDs

PD Type	Assigned Class	PSE Type	long_class_event	Minimum current IPort_MPS-2P	Minimum on time TMPS_PD	Maximum off time TMPDO_PD
3, 4	1 to 5	1, 2	FALSE	10 mA	75 ms	250 ms
		3, 4	TRUE		7 ms	310 ms

An important takeaway from this summary is that Type 3 and Type 4 PDs must still support both the 'long' timings and the AC MPS requirements when they are connected to a Type 1 or Type 2 PSE (see Table 16). The PD can recognize the PSE Type by the length of the first class event.

Table 16: AC MPS requirements per PSE and PD Type

PD Type	PSE Type	PD required to present AC MPS impedance?
All	1, 2	YES
3, 4	3, 4	NO, it is optional.

Table 17 contains the PSE IHold-2P current levels that the PSE adheres to when determining if it should continue supplying power.

Table 17: PSE IHold-2P MPS current levels

PSE Type	Assigned Class per mode	IHold-2P		TMPDO		TMPS
		Min [mA]	Max[mA]	Min [ms]	Max[ms]	[ms]
1, 2	Class 1-4	5	10	300	400	60 min
3, 4	Class 1 to 5 per pairset	2	7	320	400	6 min

9.1. PSE MPS measurements

In case of 2-pair powering (a dual-signature PD is connected to a Type 1 or Type 2 PSE), the PSE compares the current of the active pairset, IPort-2P, against IHold-2P. Type 1 and Type 2 PSEs must remove power when the amplitude of the port current is below 5 mA for longer than 400 ms. The PSE may remove power when MPS is absent for more than 300 ms.

In case of 4-pair powering (a dual-signature PD is connected to Type 3 or Type 4 PSE), Type 3 and Type 4 PSEs must remove power when the amplitude of the port current is below 2 mA for longer than 400 ms.

The PSE may remove power when MPS is absent for more than 320 ms. This applies to each pairset independently.

The PSE is required to recognize the MPS as **present** when the corresponding pair currents exceed IHold-2P max. MPS is to be recognized as **absent** when the corresponding pair current is below IHold-2P min. In all other conditions, the PSE may determine the MPS as either **present or absent**.
If there is sufficient current present for at least TMPS, followed by no more than TMPDO where current may be absent, power is maintained. If the PD fails to meet MPS for at least TMPDO, the PSE is required to remove power.

9.2. Dual-signature PD MPS design considerations

The MPS current at the PSE is measured separately for each negative pair for dual-signature PDs. The PD is required to draw at least 10 mA regardless:

a) Pair to pair unbalance that may exists at the MPS current levels.
b) Assigned class.

The requirement that a dual-signature PD has to consume 10 mA is noteworthy because, as a result of the current unbalance that a single-load dual-signature PD may generate, the PD may have to consume more than a total of 20mA over all 4-pairs in order to guarantee that each pairset will sink the required 10 mA minimum.

Bear in mind that the Type 1 / Type 2 timings have 15 ms of margin between the PD minimum on time (TMPS_PD = 75 ms) and the PSE MPS valid time (TMPS = 60 ms). With the new short timings (TMPS_PD = 7 ms) and the PSE MPS valid time (TMPS = 6 ms), that margin is only 1 ms. The PSE current level and timing have been set to take measurement accuracy into account. A PD with very low power consumption that intentionally draws MPS pulses to remain powered usually has a current sink or resistor that it can control which, together with the PD bulk capacitor and the link resistance between the PSE to the PD, forms a low pass filter that distorts the current pulse that the PSE measures. Even though the MPS current generating circuit may be activated for the correct amount of time, the time that the current sourced from the PSE effectively meets the MPS requirements may very well be lower. With the ‘short MPS’ timings, this becomes an area of attention (i.e. the PD may need to generate, as a function of its CBulk and worst-case cable length, an MPS pulse with higher amplitude, wider width, or both in order to allow a PSE to detect a 6 ms pulse width with the correct IHold-2P amplitude).

10. Summary comparison of single- and dual-signature PDs

A summary comparison of the single-signature PD and the dual-signature PD is shown in Table 18:

Table 18: Comparison of single-signature and dual-signature PDs

Parameter	Single-signature	Dual-signature
Detection signature circuitry	One for all 4 pairs	One for each pairset
Classification circuitry	One for all 4 pairs	One for each pairset
Class range	1-8	1-5 for each pairset
Mandatory classification	Yes	Yes
4PID	Yes[1]	Yes
Power demotion	Yes	Yes
PD load during power ON	Single-load	Treated as dual-load, but may be single-load
Power-up sequence	Both pairs must be ON within limited time	The 2nd pairset can be on independently from the 1st pairset
Pair to pair unbalance	IUnbalance-2P and IUnbalance_PD-2P are specified	≤ The average value of ICon_PD-2P and ≤ Pclass-2P_PD ≤ IPeak_PD-2P
Supported pair current	ICon-2P-UNB	ICon_PD-2P for PDs
MPS current	IPort_MPS: 10mA for Class 1-4 16mA for Class 5-8	IPort_MPS-2P: 10mA for Class 1-5 over each pairset
Short MPS	Yes	Yes
Autoclass	Yes	No
LLDP extensions	Yes	Yes
Switching between 2-pair and 4-pair or 4-pair and 2-pair for Class 1 to 4	Yes	No

Note 1: The knowledge that the PD is a single-signature PD is the 4PID.

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